T.O.# 33A1-10-287-1

PUBLICATION NO. 980636

1992-02M

UNIVERSAL TIMER/COUNTER

FOR INSTRUMENTS WITH REV. A (3.1) SOFTWARE

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RACAL

PUBLICATION DATE: FEBRUARY 1987

WARRANTY

Within one year of purchase, Racal-Dana will repair or replace your instrument, at our option, if in any way it is defective in material or workmanship. The instrument must be returned to the country of purchase, unless prior arrangement has been made, and Racal-Dana Instruments will pay all parts and labor charges. Just call Racal-Dana Customer Service at (714) 859-8999 in U.S.A., (0703) 843265 in England, (1) 3-955-8888 in France, 06102-2861/2 in Germany or (02) 5062767, 5052686, or 503444 in Italy for assistance. We will advise you of the proper shipping address for your prepaid shipment. Your instrument will be returned to you freight prepaid.

PROPRIETARY NOTICE

FOR YOUR SAFETY

Before undertaking any maintenance procedure, whether it be a specific troubleshooting or maintenance procedure described herein or an exploratory procedure aimed at determining whether there has been a malfunction, read the applicable section of this manual and note carefully the WARNING and CAUTION notices contained therein.

The equipment described in this manual contains voltage hazardous to human life and safety and which is capable of inflicting personal injury. The cautionary and warning notes are included in this manual to alert operator and maintenance personnel to the electrical hazards and thus prevent personal injury and damage to equipment.

If this instrument is to be powered from the AC line (mains) through an autotransformer (such as a Variac or equivalent) ensure that the common connector is connected to the neutral (earthed pole) of the power supply.

Before operating the unit ensure that the protective conductor (green wire) is connected to the ground (earth) protective conductor of the power outlet. Do not defeat the protective feature of the third protective conductor in the power cord by using a two conductor extension cord or a three-prong/two-prong adaptor.

Maintenance and calibration procedures contained in this manual sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures carefully and heed Warnings to avoid "live" circuit points to ensure your personal safety.

Before operating this instrument:

1. Ensure that the instrument is configured to operate on the voltage available at the power source. See Installation Section.

2. Ensure that the proper fuse is in place in the instrument for the power source on which the instrument is to be operated.

3. Ensure that all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If at any time the instrument:

- Fails to operate satisfactorily
- Shows visible damage
- Has been stored under unfavorable conditions
- Has sustained stress

It should not be used until its performance has been checked by qualified personnel.

AMENDMENT NO. 2 TO
PUBLICATION NUMBER 980636
MODEL 1992-02M INSTRUCTION MANUAL

1. Page 1-7, Totalize A by B specification
   Change Range specification to read:

   10^{12} -1 (Max. 9 most significant digits displayed)

2. Page 6-32, Figure 6.28

   Delete the "T-Piece" and the Digital Multimeter from illustration

3. Page 6-33, Figure 6.30

   Delete the "T-Piece" and the Digital Multimeter from illustration

T.O. 33A1-10-287-1C
Date: October 1, 1987

IDENTIFYING TECHNICAL PUBLICATION SHEET

1. PURPOSE: This technical publication is issued for the purpose of identifying and authorizing the following commercial manual for Air Force use.

MANUFACTURER: Racal-Dana Instruments Inc.

PURCHASE ORDER OR CONTRACT NO.: F41608-86-D-0294

EQUIPMENT: Model 1992/02M/04E Universal Timer/Counter

REQUISITION NO.: N/A

FEDERAL STOCK NO.: 6625-01-233-1067

TITLE: Instruction Manual 1992/02M Universal Timer/Counter

ADDITIONAL IDENTIFICATION: Covers only 02M option

DATE: First printing February 1987, Revised October 1987

2. FILE LOCATION: N/A

AMENDMENT TO
PUBLICATION NUMBER 980636
MODEL 1992-02M INSTRUCTION MANUAL

1. Add parts list for shipping kit P/N 404568 shown on page A-11 of this amendment.

2. Replace existing Figure 7.1A Final Assembly 404503 Revision B with Revision C shown on page A-5 and A-6 of this amendment.

3. Replace existing parts list for Figure 7.1A Final Assembly 404503 on page 8-4 in the Instruction Manual with the one shown on page A-11 of this amendment.

4. Add the following sub-assemblies and their parts list.

Reference Assy.			Added Sub-Assembly		Amendment Page Numbers	
P/N	Fig.	Item No.	P/N	Fig.	Drawing	Parts List
404503	7.1A	20	R-11-1728	7.1F	A-11	A-14
404503	7.1A	6	R-11-1623	7.1G	—	A-15
404506	7.1B	6	R-11-1593	7.1C	A-9	A-14
404506	7.1B	4	R-11-1592	7.1D	A-10	A-14
404506	7.1B	14	R-11-1643	7.1E	A-11	A-14
R-19-1142 (404389)	7.4	4	R-10-2891	7.4A	A-12	A-15
R-19-1142 (404389)	7.4	5	R-11-1737	7.4B	—	A-15
R-19-1145	7.6	3	R-11-1706	7.6A	A-12	A-16
401820	7.10	50	R-11-1603	7.10A	A-12	A-16

5. Add to Table 7.1 the following Suppliers:

FSC	Name
05693	Cherry Commercial Fasteners Division of Textron Inc. Santa Ana, CA
17117	Electronic Moulding Corp. Woonsocket, NJ
31223	Micro Plastics Inc. Chatsworth, CA

FSC	Name
83294	Arrow Fastener Co. Inc. Saddle Brook, NJ
92194	Alpha Wire Elizabeth, NJ
98338	Superior Radiator Minneapolis, MN
98291	Sealectro Corp. Mamaroneck, NY

6. List Part Number 404389. Channel C as an alternate to Part Number 19-1142. Refer to the following pages:

5-5	Figure 5.3
7-1	Figures 7.4 and 7.5
7-10	Title
8-1	Channel C PCB
8-5	Item 62
8-7, 8-8	Title

7. Replace existing Figure 7.1B Chassis Assembly 404506 Revision B with Revision D shown on page A-7 and A-8 of this amendment.

8. Delete Items 48, 64, 66, 100, and 130 from 404506 Chassis Assembly parts list on page 8-5. Add quantity 2 to Item 108. Add the following parts:

(12)1	R-11-1603	GPIB Plate Assy.	21793	R-11-1603
(96)2	617077	Washer, Internal Lock, #4	—	—

9. Figure 7.2, Display PCB 19-1141

   a. For clarification, the following circled numbers on the drawing should be defined:

      Item 62 is SK1,

      Item 74 is LP2,

      Item 78 is LP33

   b. Revise notes 2 and 3 to read as follows:

      2/Cut Item 64 sleeving 1/4" length and fit to LED Item 78. Heatshrink sleeve just enough to ensure retention.

      3/Cut Item 65 sleeving 1/4" length and fit to LED Items LP2, 3, 4, 5, 6, 7, 16, 22, 24, 29, 36, 42, and 45. Do **NOT** heatshrink.

   c. Change Revision Letter to "B".

10. Correct part list for Display PCB 19-1141 as follows:

   a. Change quantity of Item (4) to 1.

   b. Change Item (64)14 to (64/65)A/R.

   c. Change Revision Letter to "B".

11. Figure 7.8. Circuit Diagram. Motherboard 19-1145

    a. Change R76 from 100K to 10K.

    b. U27c on Page 7-17, lower left, change to "OR" gate by removing "circle" at pin 8.

    c. Change Revision Letter to "F".

12. Correct Motherboard 19-1145 Parts List as follows:

    a. Change R76 from Part Number R-20-5813 to R-20-5768

    Description should be : Resistor, Chip, 10K, 1/8W, 5%

    FSC: 65940 Manu P/N: MCR18-10KOHM-5 PCT

    b. Add the following parts:

Item 23	R-18-1254	Voltage Selector Card	21793	R-18-1254
Item 376	R-23-0063	Fuseholder, Top	61935	FEK-031-1666
Item 378	920204	Fuse, Slo-Blo, .50A, 250V	75915	323-500
Item 466	500215	Wire, Teflon Stranded, Grn w/Yel, 18 GA	70903	83009-DARK
Item 477	600191	Lug, Solder	83330	1416-8

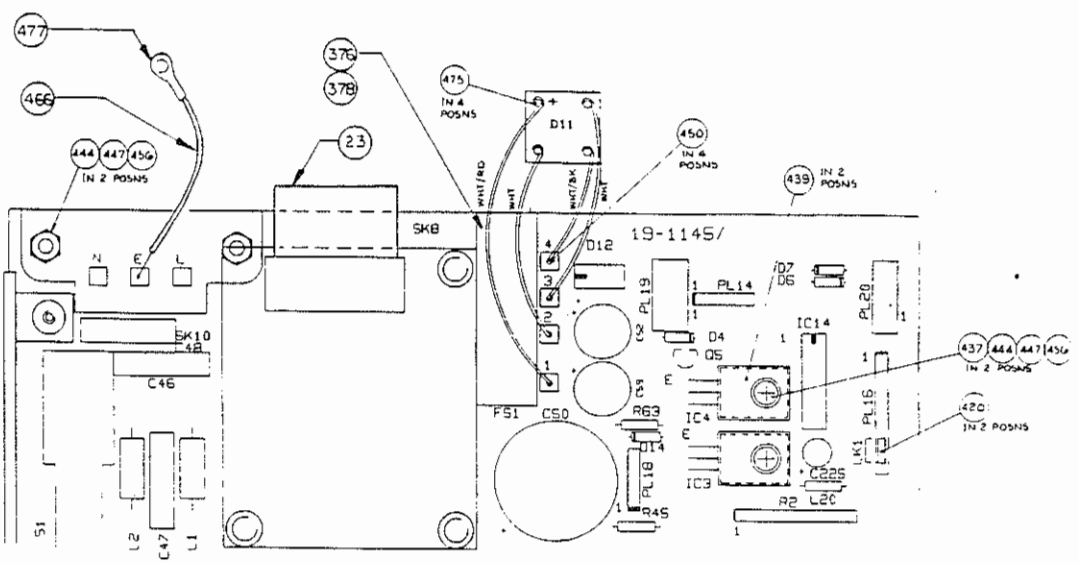
    c. Change IC24 from Part Number 230561 to 230561-001

    Integrated Circuit FSC: 21793 Manu P/N: 230561-001

    d. Change Revision Letter to "F".

13. Figure 7.6, Motherboard Layout, 19-1145

    a. Add parts listed in 12b above where shown below:



    b. Change Revision Letter to "F".

14. Figure 7.10, Component Layout. GPIB

    a. Remove Item 50.

    b. Add Note 3 below:

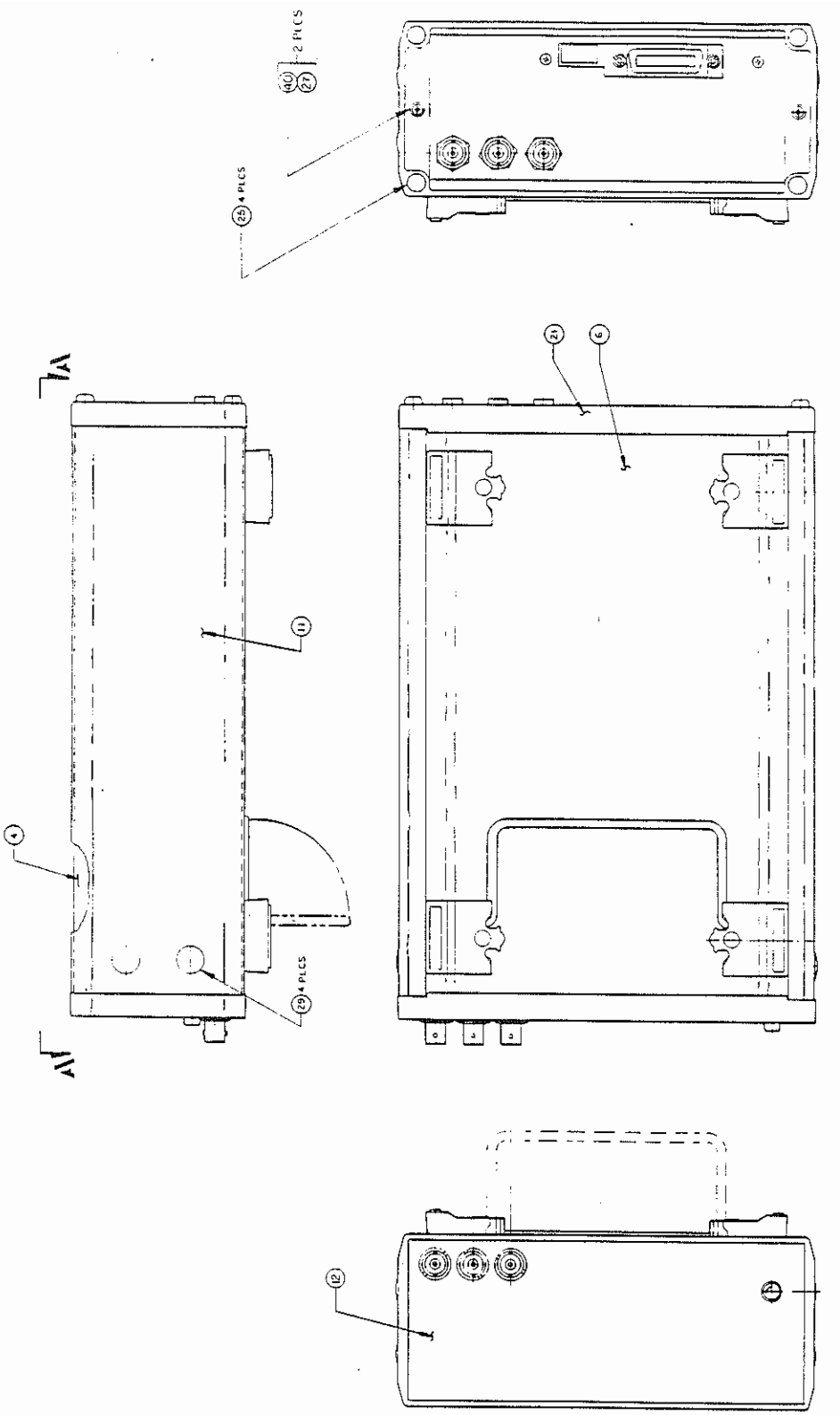
       Trim lead length of SK4 connector so that lead protrusion on PCB circuit side does not exceed 0.075 inch.

    c. Change Revision Letter to "B".

15. Page 8-15 GPIB Parts List

    a. Delete Item 50.

    b. Change Revision Letter to "B".



1- TO INSTALL GPIB PCBA, REMOVE BOTH STANDOFFS AND REPLACE AFTER FITTING BOARD TO ASSEMBLY.

NOTES: UNLESS OTHERWISE SPECIFIED.

Figure 7.1A - Final Assembly 404503 Rev. C

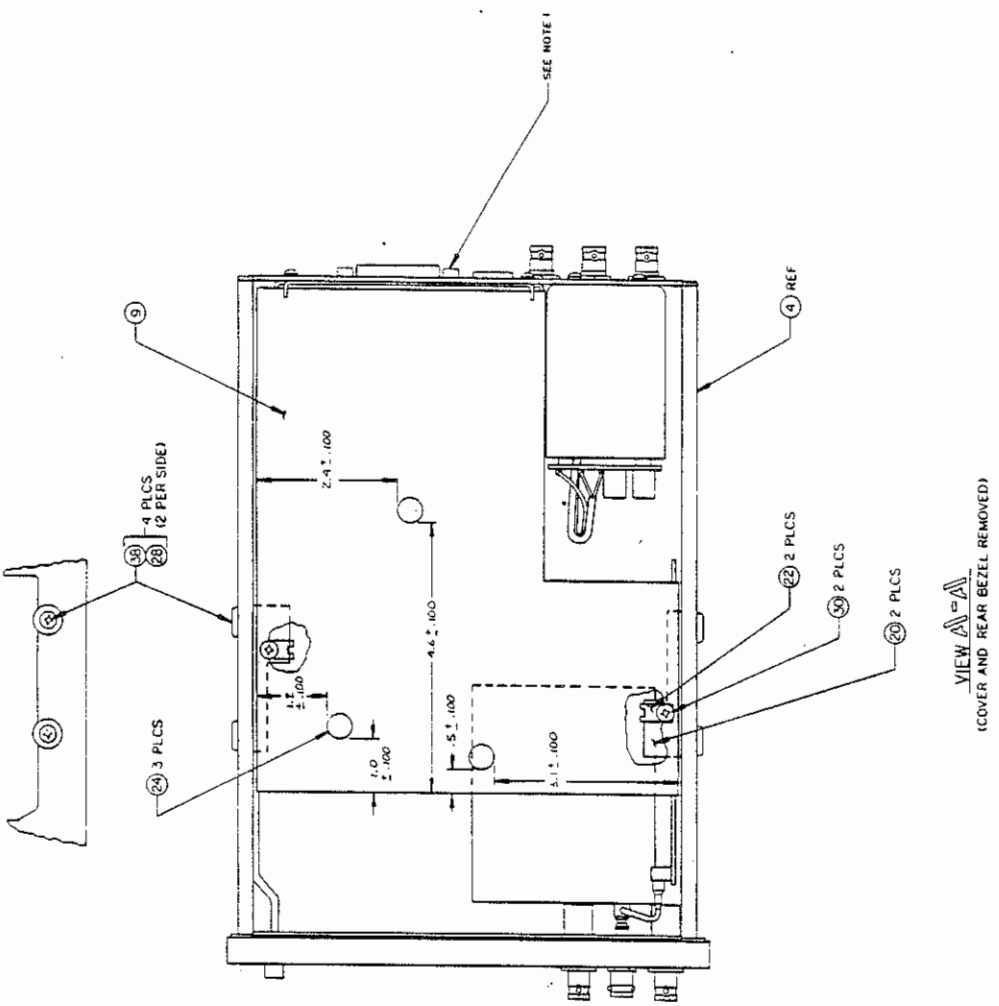


Figure 7.1A - Final Assembly 404503 Rev. C (Cont'd)

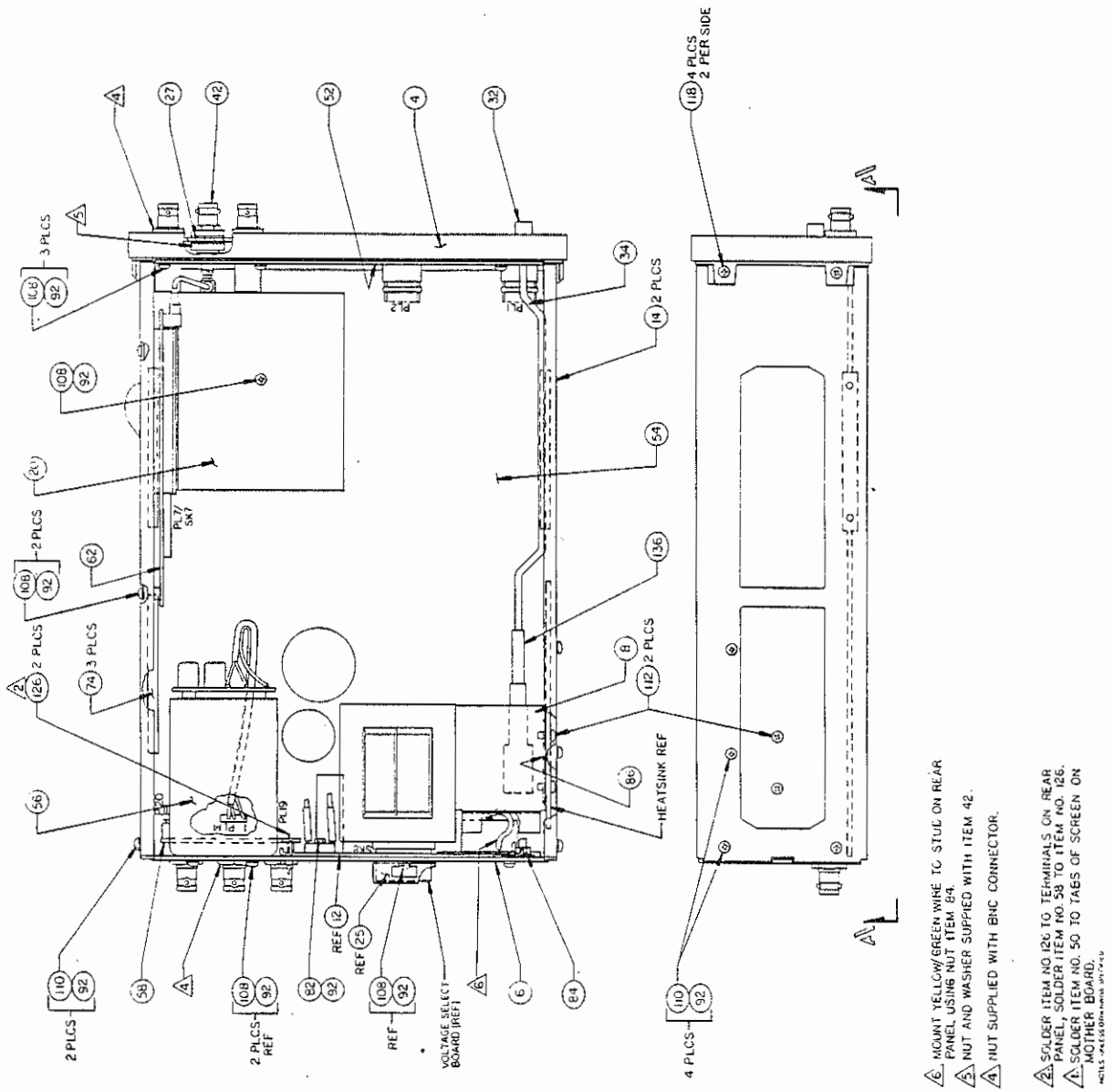


Figure 7.1B - Chassis Assembly 404506 Rev. D

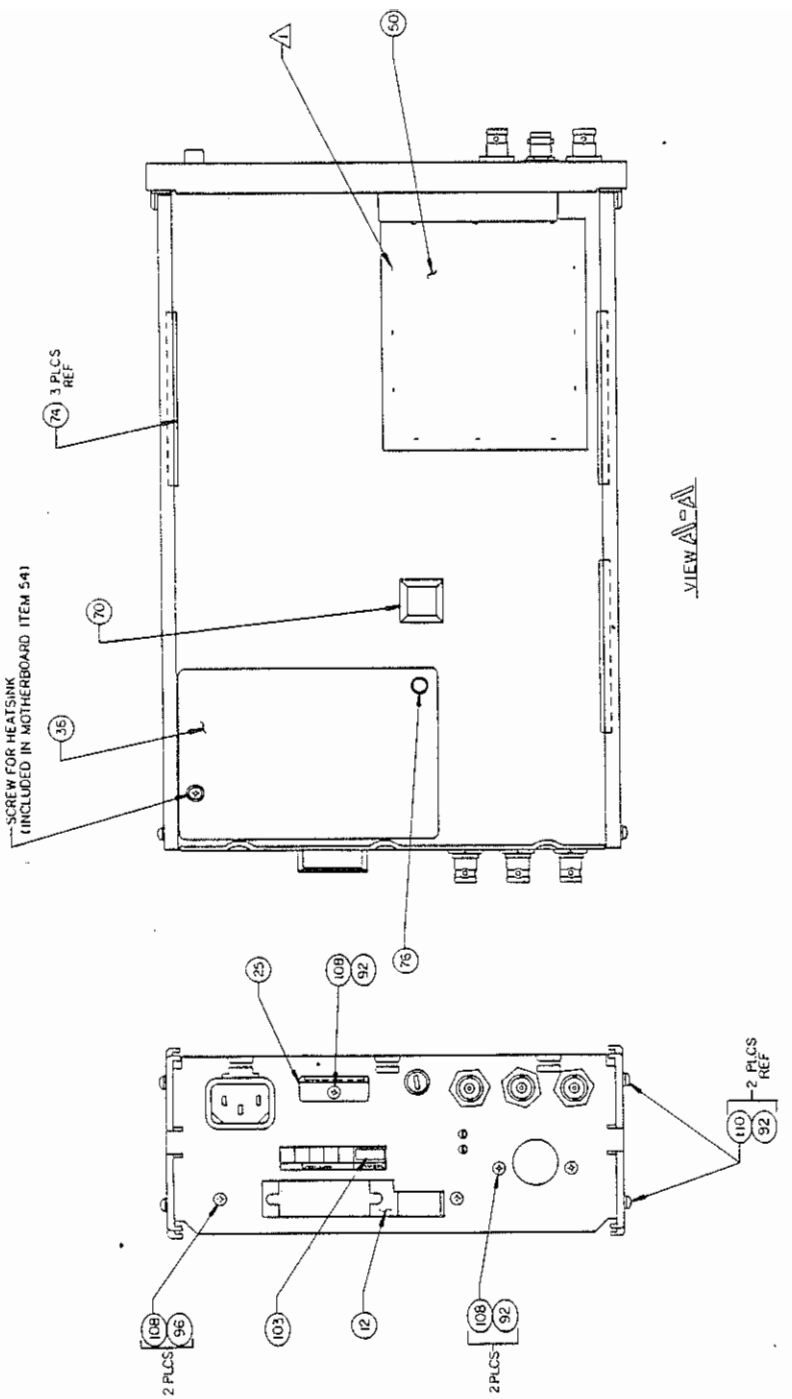


Figure 7.1B - Chassis Assembly 404506 Rev. D (Cont'd)

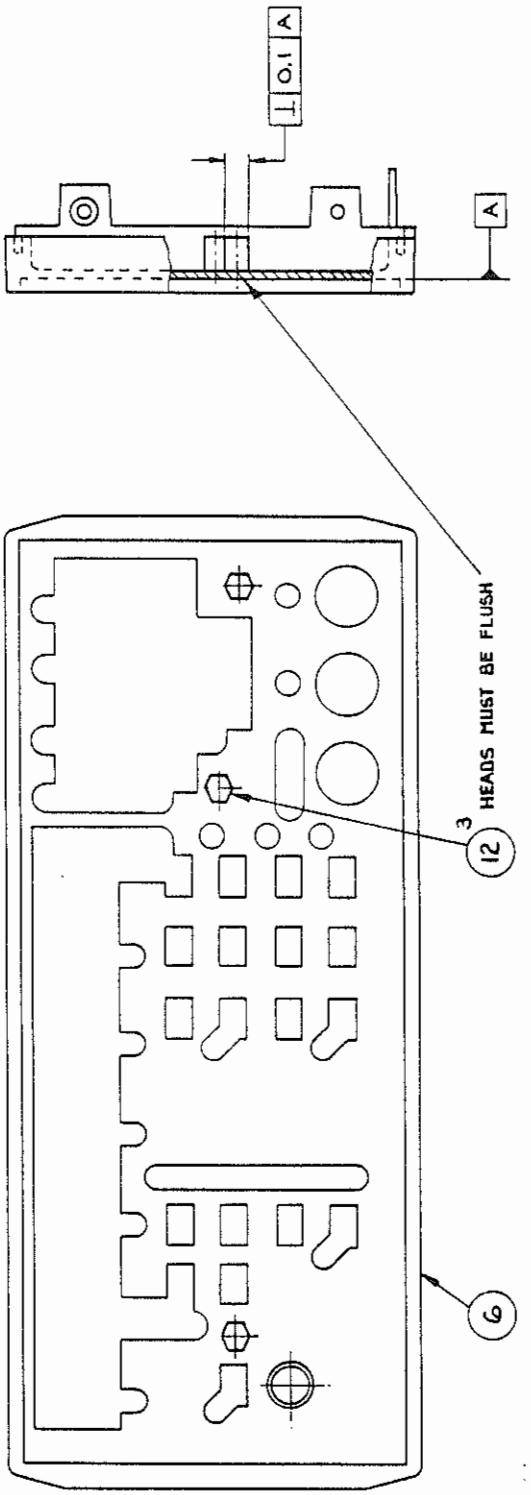


Figure 7.1C - Front Panel Sub-Assy R-11-1592 Rev. 3

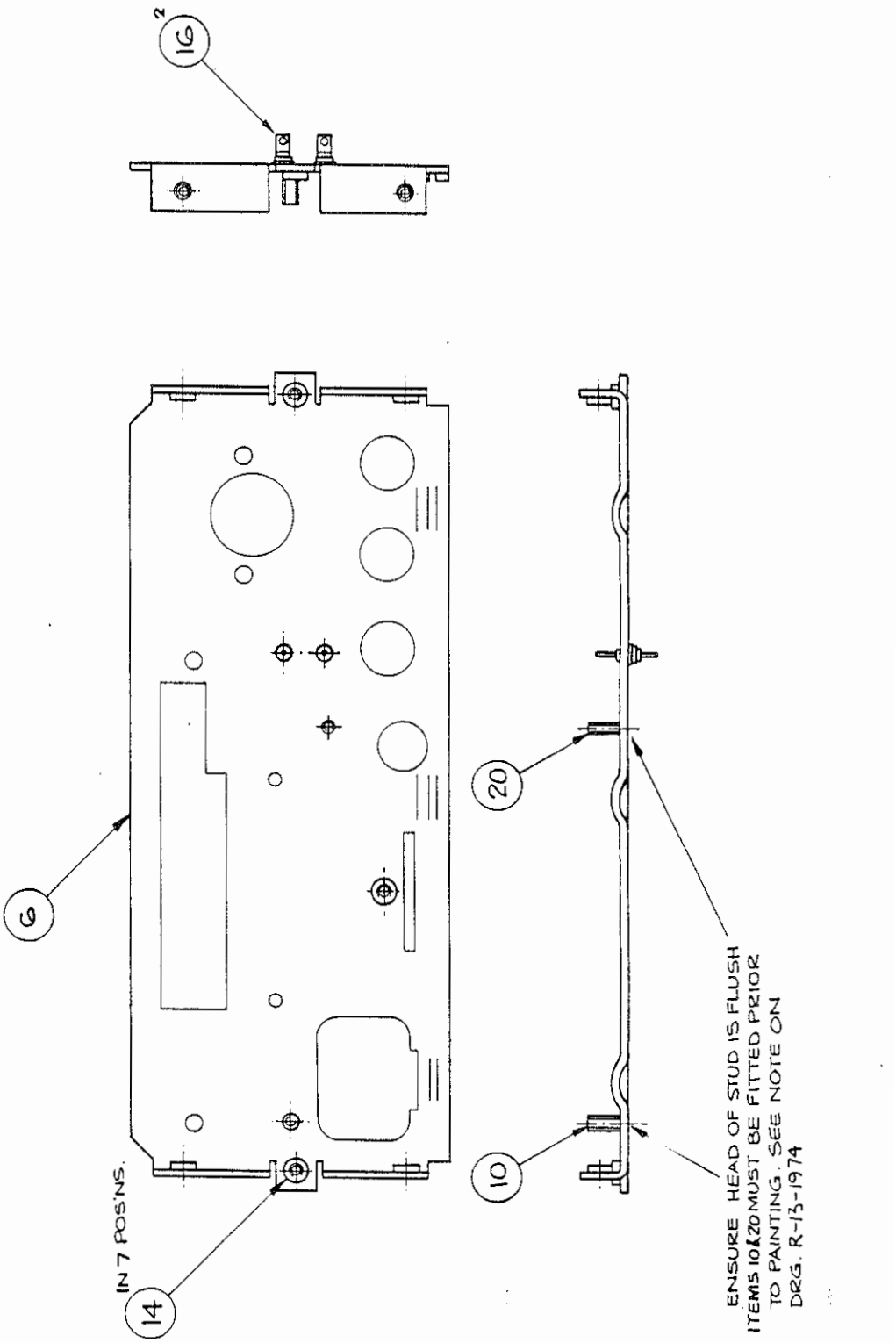


Figure 7.1D - Rear Panel Sub-Assy R-11-1593 Rev. A

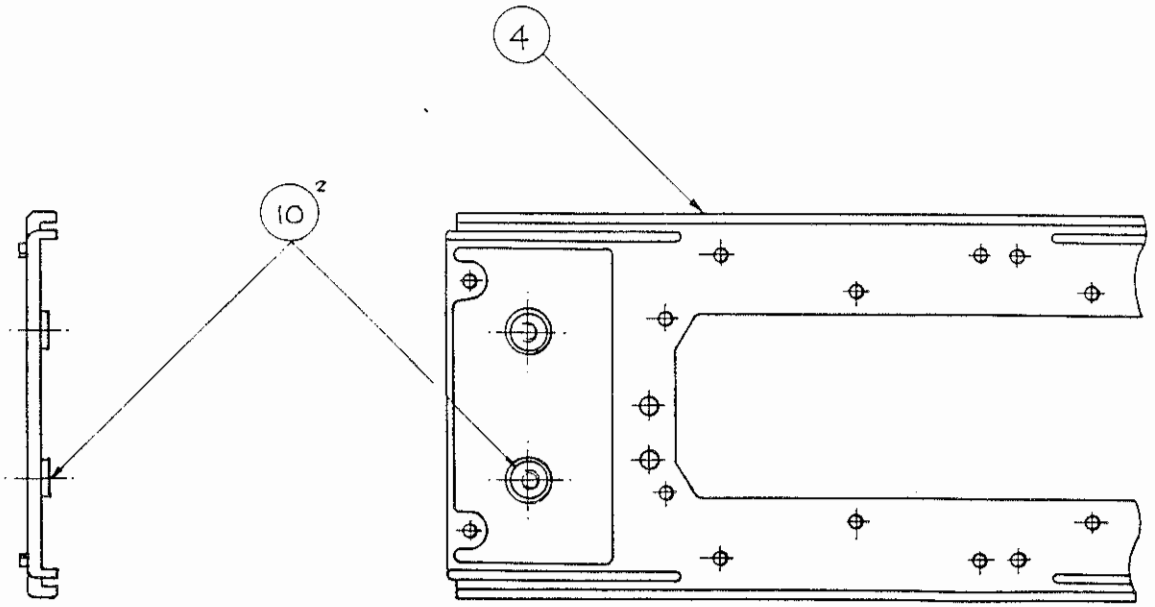


Figure 7.1E - Side Panel Assy R-11-1643 Rev. 1

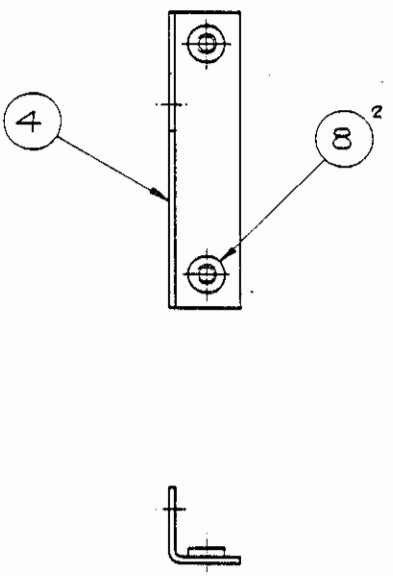


Figure 7.1F Bracket Assembly R-11-1728 Rev. 1

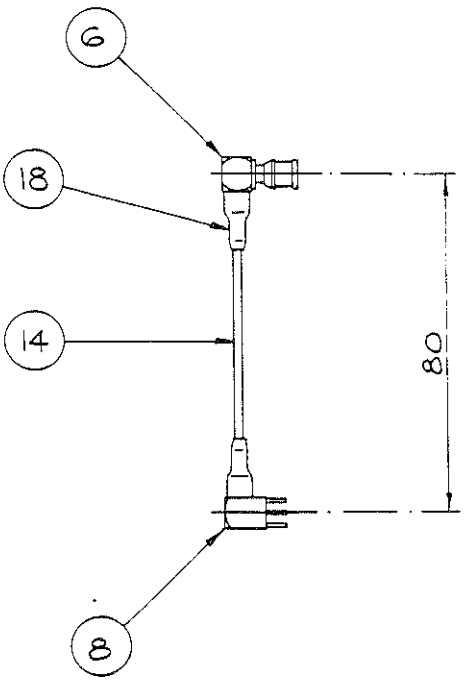


Figure 7.4A - Coax Cable Assy R-10-2891 Rev. A

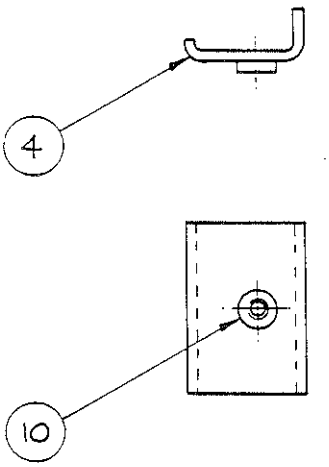


Figure 7.6A - Clamp Assy R-11-1706 Rev. 1

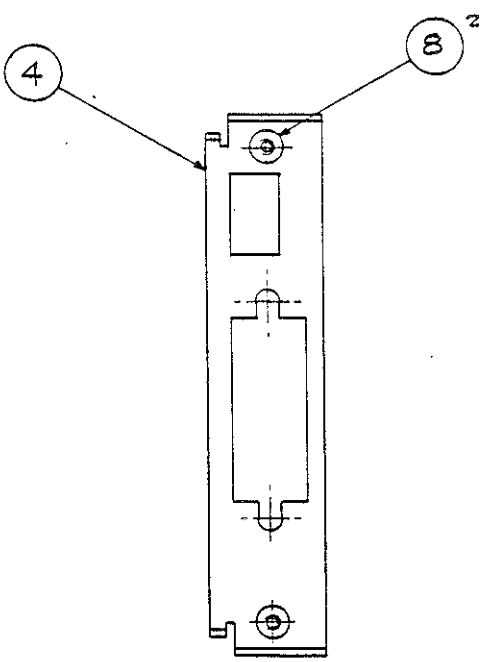


Figure 7.10A - GPIB Plate Assy R-11-1603 Rev. 1

404568, SHIPPING KIT, REV. A, FIGURE 7.1

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
1	980636	MANUAL, INSTRUCTION	21793	980636
2	920756	FUSE, .25 AMP, 250V	75915	313R250A
3	R-23-0066	FUSE, 1/8 AMP	21793	R-23-0066
4	600620	CABLE ASSY., POWER	70903	17250B

404503, FINAL ASSEMBLY, REV. C FIGURE 7.1A

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
(4)1	404506	CHASSIS ASSY.	21793	404506
(6)1	R-11-1623	BOTTOM COVER ASSY.	21793	R-11-1623
(9)1	401820	PCB ASSY., GPIB	21793	401820
(11)1	R-13-1972	COVER, FORMED	21793	R-13-1972
(12)1	R-13-1976	OVERLAY, FRONT PANEL	21793	R-13-1976
(20)2	R-11-1728	BRACKET ASSY.	21793	R-11-1728
(21)1	R-15-0672	BEZEL, REAR	21793	R-15-0672
(22)2	R-24-0146	"U" NUT	K8918	SNU-2811-17-4
(24)3	R-24-0245	BUTTON, RUBBER	53387	SJ-5003 BLACK
(25)4	R-24-0250	FASTENER, PUSH-IN	31223	27P1F0051 BLACK
(27)2	R-24-2801	WASHER, CRINKLE, M3	21793	R-24-2801
(28)4	R-24-2816	WASHER, NYLON	13764	11SFW0008 NAT
(29)4	R-24-7042	GROMMET, BLIND, GRAY	21793	R-24-7042
(30)2	R-24-5835	SCREW, #6AB X .375	21793	R-24-5835
(38)4	R-24-7543	SCREW CSKHD, M4 X 10	21793	R-24-7543
(40)2	R-616315	SCREW, PAN HD, M3 X 6	83294	7985-A-M3X6MM

R-11-1592, FRONT PANEL SUB-ASSY., REV. 3, FIGURE 7.1C

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
(6)1	R-15-0673	CASTING, FRONT PANEL	21793	R-15-0673
(12)3	R-24-4086	STANDOFF, M3 X 9	46384	PTSO-0030-9MM

R-11-1593, REAR PANEL SUB-ASSY., REV. A, FIGURE 7.1D

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
(6)1	R-13-1974	REAR PANEL	21793	R-13-1974
(10)1	R-24-2221	CAPTIVE STUD, M4 X 10	46384	FH-M4-10-CI
(14)7	R-24-2243	FASTENER, SELF-CINCHING	46384	S-M3-2-CI
(16)2	601360	TERMINAL, FEED-THRU	17117	4338-67-1
(20)1	R-24-2232	CAPTIVE STUD, M3 X 12	46384	FH-M3-12-CI

R-11-1643, SIDE PANEL ASSY., REV. 1, FIGURE 7.1E

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
(4)1	R-15-0671	CASTING, SIDE PANEL	21793	R-15-0671
(10)2	R-24-2248	FASTENER, SELF-CINCHING, M4	46384	S-M4-3-CI

R-11-1728, BRACKET ASSY., REV. 1, FIGURE 7.1F

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
(4)1	R-13-2095	BRACKET, SUPPORT	21793	R-13-2095
(8)2	R-24-2246	FASTENER, SELF-CINCHING, M4	21793	R-24-2246

R-11-1623, BOTTOM COVER ASSY., REV. A, FIGURE 7.1G

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
(4)1	R-13-1973	COVER, BOTTOM	21793	R-13-1793
(8)1	R-15-0675	BAIL	21793	R-15-0675
(18)4	610554	SCREW, #8B X .375	21793	610554
(20)A/R	920504	ADHESIVE, SCOTCH GRIP	21793	920504
(22)4	454621	FOOT, BOTTOM	21793	454621
(24)4	454355	INSERT, RUBBER	21793	454355
(26)4	920958	INSERT, RUBBER	98338	3188

R-10-2891, COAX CABLE ASSY., REV. A, FIGURE 7.4A

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
(6)1	R-23-3378	PLUG, RIGHT ANGLE	98291	51-0328-3196-22
(8)1	R-23-3427	TERMINATOR, RIGHT ANGLE	21793	23-3427
(14)1	500254	CABLE, COAXIAL	92194	9178B
(18)1	500002	SLEEVING, HEATSHRINK	29005	RNF-100-1-3/16

R-11-1737, LID ASSY., REV. A, FIGURE 7.4B

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
(10)1	R-13-2104	LID	21793	R-13-2104
(20)1	455134	STRIP, CONTACT, SINGLE	21793	23-9159
(26)1	R-24-3150	RIVET	05693	AAP-41

R-11-1706, CLAMP ASSY., REV. 1, FIGURE 7.6A

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
(4)1	R-13-2073	CLAMP ASSY.	21793	R-13-2073
(10)1	R-24-2247	FASTENER, SELF-CINCHING, M4	46384	S-M4-2-CI

R-11-1603, GPIB PLATE ASSY., REV. 1, FIGURE 7.10A

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
(4)1	R-13-2004	BRACKET	21793	R-13-2004
(8)2	R-24-2243	FASTENER, SELF-CINCHING, M3	21793	R-24-2243

16. **Page 5-13**. Subsection 5.3.5.2.3

    Change IC2 to read IC1-b (2 places).

17. **Page 6-13**, Figure 6.11 - Fault Finding Flowchart - Part 1

    Change Q20 and Q19 EMITTER (power supply points) to read IC3 and IC4 OUTPUT, respectively.

18. **Page 6-14**, Figure 6.11 - Fault Finding Flowchart - Part 1

    Change >200 ms to read >350 ms for the reset signal at IC19-1.

19. **Page 6-29**, Subsection 6.7.4.2.C

    Change signal generator level of 5.0 mV RMS to read 8.0 mV RMS.

20. **Page 6-29**, Subsection 6.7.4.2.e

    Change output level of 4.5 mV RMS to read 7.5 mV RMS.

21. **Page 6-37**, Subsection 6.9.9.2.C

    Change 12V peak-to-peak to read 10V peak-to-peak.

22. **Page 6-38**, Figure 6.36 - Trigger Level Waveform

    Change interval of displayed waveform from ~600 µs to ~600 ms.

23. **Page 6-39**, Table 6.9 - Internal Frequency Standard Accuracy

    a. For Display, change ± 10 E-3 to read ± 300 E-3

    b. For Accuracy, change 1 part in 10^9 to read 3 parts in 10^8

24. **Page 8-8**, Channel C Parts List - R27

    Change FSC to: 73138 and Manu P/N to: 72XLR20K

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LIST OF ILLUSTRATIONS

LIST OF TABLES

Manual Revisions and Changes

Any revisions or changes to this manual will be listed separately and located at the rear of this manual. Actions called for by these revisions or changes should be executed as soon as possible.

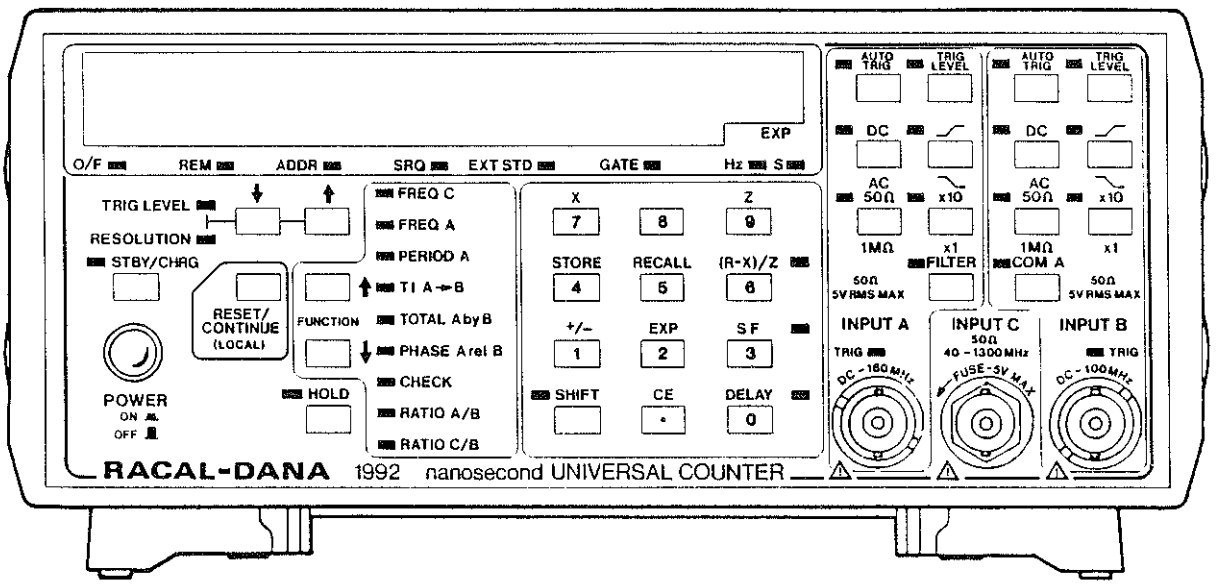


Figure 1.1 - Model 1992-02M Universal Timer/Counter

SECTION 1 GENERAL INFORMATION

1.1 INTRODUCTION

1.1.1 This Instruction Manual provides information for installing, operating, and servicing of Racal-Dana's MATE Frequency/Time Interval Meter (FTIM) 1992-02M. The designation 1992-02M is used throughout this manual. Figure 1.1 (facing page) shows a front view of the 1992-02M. The 1992-02M offers universal counter functions using Inputs A and B. The 1992-02M also provides frequency measurements to 1.3 GHz using Input C.

1.2 SUMMARY

1.2.1 This manual is organized into the following eight sections:

SECTION 1. General Information:

a. Published Specifications

b. Safety

c. Product Support

d. General Description

SECTION 2. Installation and Preparation for Use:

a. Unpacking and Initial Inspection

b. Reshipment

c. Power Connections

d. Storage and Temperature

e. Functional Check

f. Miscellaneous Setup Procedures

g. GPIB Preparation for Use

SECTION 3. Local Operation:

a. Panel Descriptions

b. Measurement Procedures

c. General Operating Information

SECTION 4. System Operation

SECTION 5. General Theory of Operation

SECTION 6. Maintenance:

a. PVP/Calibration Inspection Intervals

b. Required Test Equipment

c. Dismantling and Reassembly

d. Special Functions for Diagnostic Purposes

e. Troubleshooting

f. Post-Repair Setup

g. Internal Frequency Standard - Routine Calibration

h. Overall Performance Verification Procedure

SECTION 7. Drawings:

a. Assembly Drawings

b. Schematic Drawings

SECTION 8. Parts List:

a. Replaceable Parts and Assemblies

1.3 SPECIFICATIONS

1.3.1 Table 1.1 lists the 1992-02M specifications. The specifications indicate the performance standards to which the instrument conforms at the time of shipment.

Table 1.1 - 1992-02M Specifications

INPUT CHARACTERISTICS	
Inputs A and B	
Frequency Range:	
Input A:	DC to 160 MHz DC-coupled 10 Hz to 160 MHz AC-coupled
Input B:	DC to 100 MHz DC-coupled 10 Hz to 100 MHz AC-coupled
Sensitivity:	
Sine Wave:	25 mV rms DC to 100 MHz 50 mV rms to 160 MHz
Pulse:	75 mV p-p, 5 ns min. width
Dynamic Range: **(x1 attenuation)**	75 mV to 5V p-p to 50 MHz 75 mV to 2.5V p-p to 100 MHz 150 mV to 2.5V p-p to 160 MHz
Signal Operating Range:	
x1 attenuation:	± 5.1V
x10 attenuation:	± 51V
Input Impedance (nominal):	
(x1 and x10 attenuation)	
Separate Mode:	50 ohms or 1 Megohm // ≤45 pF
Common Mode:	50 ohms or 1 Megohm // ≤55 pF
Maximum Input (without damage):	
50 ohms:	5V (DC + AC rms)
1 Megohm: **(x1 attenuation)**	260V (DC + AC rms), DC to 2 kHz Decreasing to 5V rms, at 100 kHz and above
1 Megohm: **(x10 attenuation)**	260V (DC + AC rms), DC to 20 kHz Decreasing to 50V rms at 100 kHz and above
Coupling:	AC or DC
Low Pass Filter:	50 kHz nominal (Input A selectable)
Trigger Slope:	+ve or -ve
Attenuator:	x1 or x10. In Auto Trigger mode, attenuator selected automatically if necessary

Table 1.1 - 1992-02M Specifications (Cont'd)

Trigger Level Range:	
Manual:	
x1 attenuation:	± 5.1V in 20 mV steps
x10 attenuation:	± 51V in 200 mV steps
Automatic:	± 51V
Trigger Level Accuracy:	
Manual and Automatic:	
x1 attenuation:	± 30 mV ±1% of trigger level reading
x10 attenuation:	± 300 mV ±1% of trigger level reading
Auto Trigger:	
Frequency Range:	DC and 50 Hz to 100 MHz (Typically 160 MHz)
Min. Amplitude (AC):	Typically 150 mV p-p*
x10 attenuator	Automatically selected if input signal exceeds ± 5.1V or 5.1V p-p*
Trigger Level Outputs: (Rear Panel)	
Range:	± 5.1V
Accuracy (Relative to true trigger level)	
x1 attenuation:	± 1% V output ±10 mV
x10 attenuation:	± 1% V output ± 100 mV
Impedance:	10 kohm nominal
Input C	
Frequency Range:	40 MHz to 1.3 GHz
Sensitivity:	
Sine Wave:	<15 mV rms, 40 MHz to 1 GHz <75 mV rms to 1.3 GHz
Dynamic Range:	15 mV rms to 5V rms to 1 GHz 75 mV rms to 5V rms to 1.3 GHz
Input Impedance:	50 ohms nominal AC-coupled
VSWR:	≤2:1 at 1 GHz
Maximum Input:	7V rms (fuse-protected) Fuse located in BNC connector
Damage Level:	2.5W

*See Definitions

Table 1.1 - 1992-02M Specifications (Cont'd)

MEASUREMENT MODES	
Frequency A	
Range:	DC to 160 MHz
Digits Displayed:	3 to 9 digits plus overflow
LSD Displayed (Hz):	$F \times 10^{-D}$ (D = No. of digits, F = Frequency rounded up to next decade)*
Resolution* (Hz):	± LSD† ± (Trig. Error* x Frequency) /Gate Time
Accuracy* (Hz):	± Resolution ± (Timebase Error x Frequency)
Frequency C	
Range:	40 MHz to 1.3 GHz
LSD*:	As for Frequency A
Resolution* and Accuracy*:	As for Frequency A
Time Interval	
Range:	
Separate Mode:	0 to 8×10^5s Typically -2 ns to $+8 \times 10^5$s
Common Mode:	5 ns to 8×10^5s
Input:	
Common:	Input A START and STOP
Separate:	Input A START Input B STOP
Trigger Slopes:	+ve or -ve Selectable START and STOP
LSD Displayed:	1 ns min
Resolution* (sec):	± LSD ± 1 ns ± Trig Error*
Accuracy* (sec):	± Resolution ± (Timebase Error x T1) ± Trigger Level Timing Error* ± 2 ns**

*See Definitions
†2LSD for 6-9 digits displayed
**A differential delay which may be reduced by numerical offset or external compensation.

Table 1.1 - 1992-02M Specifications (Cont'd)

Time Delay	
Available on Time Interval and Totalize	
Range:	200 µs to 800 ms nominal
Step Size:	25 µs nominal
Accuracy:	± 0.1% Rdg. ± 50 µs
Period A	
Range:	6.25 ns to 1.7×10^3s
Digits Displayed:	3 to 9 digits plus overflow
LSD Displayed (sec):	$P \times 10^{-D}$ (D = No. of digits, P = Period rounded up to next decade)*
Resolution* (sec):	± LSD† ± (Trig. Error* x Period) /Gate Time
Accuracy* (sec):	± Resolution ± (Timebase Error x Period)
Ratio A/B	
Specified for higher frequency applied to Input A	
Range:	DC to 100 MHz on both inputs
LSD Displayed: (for 6-9 digits selected)	$\left(\frac{10}{\text{Freq. B x Gate Time}}\right)$, rounded to nearest decade*
Resolution*:	± LSD ± (Trig. Error B*/Gate Time) x Ratio
Accuracy*:	± Resolution
Ratio C/B	
Specified for higher frequency applied to Input C	
Range:	Input C 40 MHz to 1.3 GHz Input B DC to 100 MHz

*See Definitions
†2LSD for 6-9 digits displayed

Table 1.1 - 1992-02M Specifications (Cont'd)

LSD Displayed: **(for 6-9 digits selected)**	$\left(\frac{640}{\text{Freq. B x Gate Time}}\right)$, rounded to nearest decade*
Resolution* and Accuracy*:	As for Ratio A/B
Totalize A by B	
Accumulative or single totalize	
Input:	Input A
Range:	10^{18}-1 (Max. 9 most significant digits displayed)
Maximum Rate:	10^{8} events/s
Minimum Pulse Width:	5 ns min. at trigger points
Accuracy:	± 1 count
Start/Stop:	Electrical (Input B) or Manual
Phase (A rel. to B)	
Range:	0.1° to 360°
LSD Displayed:	0.1° to 1 MHz 1.0° to 10 MHz 10° to 100 MHz
Resolution* (degrees):	± LSD ± (TI Resolution/Period A) x 360°
Accuracy* (degrees):	± LSD ± (TI Accuracy/Period A) x 360°
Amplitude Measurement	
Peak*	
Frequency Range:	50 Hz to 20 MHz
Amplitude Range:	160 mV p-p to 51V p-p
Resolution:	
x1 attenuation:	20 mV
x10 attenuation:	200 mV
Accuracy:	
x1 attenuation:	± 50 mV ± 6%V p-p (Typically ± 40 mV ± 2%V p-p)
x10 attenuation:	± 500 mV ± 10%V p-p (Typically ± 400 mV ± 3%V p-p)

*See Definitions

Table 1.1 - 1992-02M Specifications (Cont'd)

DC (< 15 mV p-p AC)	
Amplitude Range:	± 51V
Resolution:	
x1 attenuation:	20 mV
x10 attenuation:	200 mV
Accuracy:	
x1 attenuation:	± 40 mV ± 1% Rdg.
x10 attenuation:	± 400 mV ± 1% Rdg.

Math

Available on all measurements except Phase and Check

Function:	(Result - X)/Z
Entry Range:	$\pm 1 \times 10^{-10}$ to $\pm 1 \times 10^{10}$ to 9 significant figures

EXTERNAL ARMING

A comprehensive external arming capability to determine the START and/or STOP point of a measurement. Available on all measurement functions except phase.

Input Signal: (via Rear Panel)	TTL compatible (min. pulse width 200 ns)
Slope:	+ve or -ve independently selectable on START or STOP arm
Impedance:	1 kohm nominal

GENERAL SPECIFICATIONS

Internal Timebase:

High-Stability Oven Oscillator 04E, a proportionally controlled ovenized Internal Frequency Standard

Frequency:	10 MHz
Aging:	$< 5 \times 10^{-10}$ per day at time of shipment
Temperature Stability:	$< 7 \times 10^{-9}$ over the range 0°C to 50°C
Line Voltage Stability:	$< 5 \times 10^{-10}$ two minutes after a 10% line voltage change

Frequency Standard Output:	
Frequency:	10 MHz
Amplitude:	> 600 mV p-p into 50 ohms
Impedance:	250 ohms nominal

Table 1.1 - 1992-02M Specifications (Cont'd)

External Standard Input:	
Frequency:	10 MHz
Signal Amplitude:	Min. 100 mV rms
(Sine Wave)	Max. 10V rms
Impedance:	1 kohm nominal at 1V p-p 500 ohms nominal at 10V p-p
Gate Time:	
(Frequency, Period, and Ratio modes)	Automatically determined by resolution selected (Range 1 ms - 10s)*

Resolution Selected:	Gate Time: (seconds)
9 + overflow	10
9	1
8	0.1
7	0.01
6,5,4,3	0.001

Single Cycle:	Enables a single measurement to be
(Hold)	initiated and held
Display:	9-digit, high brightness, 14 mm LED display in engineering format with exponent digit
Power Requirements:	
Voltage:	90-110 103-127 193-237 207-253 VAC
Frequency:	45-450 Hz
Rating:	35 VA max.
Environmental Requirements:	
Temperature, Storage:	-40°C to +75°C
Temperature, Operating:	0°C to +50°C
Relative Humidity:	95% to 30°C 75% to 40°C 45% to 50°C
Altitude, Storage:	12,000 meters
Altitude, Operating:	3,050 meters
Vibration:	2 g
Shock:	30 g

*See Definitions

Table 1.1 - 1992-02M Specifications (Cont'd)

Safety:	Designed to meet the requirements of IEC 348 and follow the guidelines of UL1244
Weight:	Net 3.63 kg (8 lb) Shipping 5.5 kg (11 lb)
Dimensions, Instrument:	331 x 212 x 88 mm (13.03 x 8.35 x 3.46 in)

SUPPLIED ACCESSORIES

Power Cord
Instruction Manual
230V Operation Fuse (.25A)

ORDERING INFORMATION

1992-02M Universal Timer/Counter with MATE Interface

DEFINITIONS

LSD (Least Significant Digit)
In Frequency and Period modes display automatically upranges at 1.1 x decade and downranges at 1.05 x decade, except on Input C for input frequency >1 GHz

Accuracy and Resolution Expressed as an RMS value

Trigger Error RMS

$$\text{Trigger Error (seconds)} = \sqrt{\frac{(e_{i1}^2 + e_{n1}^2)}{S1^2} + \frac{(e_{i2}^2 + e_{n2}^2)}{S2^2}}$$

where e_i = input amplifier RMS noise (typically 150 µV RMS in 160 MHz bandwidth)
e_n = input signal RMS noise in 160 MHz bandwidth
S = Slew rate at trigger point V/s
Suffix 1 denotes START edge
Suffix 2 denotes STOP edge
In Frequency A, Period A, Frequency B and Period B modes, triggering is always on positive-going edge

Trigger Level Timing Error

$$\text{Trigger Level Timing Error (seconds)} = 0.035\left(\frac{1}{S1} - \frac{1}{S2}\right)$$

$$\text{typically} = 0.018\left(\frac{1}{S1} - \frac{1}{S2}\right)$$

S1 = Slew rate on START edge V/s
S2 = Slew rate on STOP edge V/s

Table

Gate Time

The nominal gate time indicated is set by the resolution selected in Frequency, Period, Ratio, and Check modes. It is the value which is used in the calculation of LSD and Resolution. The true gate time will be extended from this value by up to:

(a). One period of the input signal(s) on Frequency B, Period B, and Ratio A/B

(b). Two periods of the input signal on Frequency A and Period A

(c). One period of input signal B on Ratio C/B

Peak and Peak-to-Peak Amplitudes

Peak is defined as being the highest or lowest point at which the signal width is 5 ns. Similarly, Peak-to-Peak is the difference between the highest and lowest points at which the signal width is 5 ns.

1.4 SAFETY

1.4.1 The 1992-02M incorporates a protective earth terminal and is designed to meet international safety requirements. Refer to the Safety Page "FOR YOUR SAFETY" immediately preceding the Table of Contents. Follow all **NOTES**, CAUTIONS, and **WARNINGS** to ensure personal safety and prevent damage to the instrument.

1.5 PRODUCT SUPPORT

1.5.1 Racal-Dana supports the 1992-02M with Product Engineering, Service, and Parts Departments. A complete listing of service centers and field representatives is provided on the last two pages of the manual.

1.6 GENERAL DESCRIPTION

1.6.1 The 1992-02M is a universal timer/counter designed for system or bench use. Basic measurement functions (described briefly in Subsection 1.6.2) include Frequency, Period, Time Interval, Totalize, Phase, and Ratio.

1.6.2 Measurement Functions

1.6.2.1 Frequency A Function

1.6.2.1.1 Frequency A function is used to measure the frequency of the signal applied to the Channel A input. A resolution of nine digits is available with a one-second gate time.

1.6.2.2 Frequency B Function

1.6.2.2.1 Special Function 21 (see Subsection 3.8 "Special Functions"), permits Frequency B measurements. Frequency B function is used to measure the frequency of the signal applied to the Channel B input. A resolution of nine digits is available with a one-second gate time.

1.6.2.3 Frequency C Function

1.6.2.3.1 Frequency C function is used to measure the frequency of the signal applied to the Channel C input. A resolution of nine digits is available with a one-second gate time.

1.6.2.4 Period A Function (See Note below)

1.6.2.4.1 Period A function is used to measure the period of the waveform applied to the Channel A input. A number of periods, depending upon the resolution (and, therefore, the gate time) selected, are measured and the average value is displayed.

1.6.2.5 Time Interval Function A→B (See Note below)

1.6.2.5.1 Time Interval function is used to perform single-shot measurements of the time interval between:

a. An event occurring at the Channel A input and a later event at the Channel B input (using separate input channels)

b. Two events occurring at the Channel A input (using a common input channel)

1.6.2.5.2 The arming of the stop circuit can be delayed for a specific time set by the operator. This feature prevents the measurement interval being stopped prematurely by spurious pulses, such as those caused by relay contact bounce.

1.6.2.6 Total A Function (See Note next page)

1.6.2.6.1 Total A function permits events occurring at the Channel A input to be totalized. The counting interval can be controlled by:

a. Electrical start and stop signals applied to the Channel B input (Total A by B)

b. Successive operations of a front-panel key (Manual Totalize)

1.6.2.6.2 Delayed arming of the stop circuit to prevent spurious triggering is available in the Total A by B measurement mode. The Manual Totalize mode provides the capability for totalizing cumulatively over a number of periods.

1.6.2.7 Phase A rel B Function (See Note next page)

1.6.2.7.1 Phase A rel B function is used to measure the phase difference between the waveform applied to the Channel A input and that applied to the Channel B input. The phase difference is displayed in degrees, and indicates the phase lead at the Channel A input. The signals for phase measurement must be continuous and have the same frequency.

1.6.2.8 Ratio A/B Function

1.6.2.8.1 Ratio A/B function is used to measure the ratio of the frequency applied to the Channel A input to that applied to the Channel B input.

1.6.2.9 Ratio C/B Function

1.6.2.9.1 Ratio C/B function is used to measure the ratio of the frequency applied to the Channel C input to that applied to the Channel B input.

NOTE:

Special Function 21 (see Subsection 3.8 "Special Functions") permits Period B, Time Interval B→A, Total B by A, and Phase B rel A. For these functions, note the following:

a. Period B is specified down to 10 ns

b. Total B by A operates for one complete cycle of the Channel A signal. The stop circuit delay is available on Channel A

1.6.3 Check Function

1.6.3.1 With the Check function selected, a number of functional tests of the instrument's circuits can be made without the use of additional test equipment. Although these tests do not check the instrument's performance to published specifications, they can be used to verify that the equipment is operating correctly following receipt or transportation to a new location. A brief, preliminary functional check procedure is given in Section 2.

1.6.4 Input Signal Channels

1.6.4.1 Inputs A and B are fully independent. However, provision is made for connection of the signal at the Channel A input into both channels. This is effected by selecting the COM(mon) A mode. When COM A is selected, Channel B's input socket is isolated from Channel B's circuitry.

1.6.4.2 Inputs A and B are provided with independent controls to permit the following selections:

a. AC or DC input coupling

b. 1MΩ or 50Ω input impedance

c. x1 or x10 input attenuation

d. positive or negative-slope trigger

e. manually or automatically-set input trigger level

1.6.4.2.1 The manually-set trigger level is entered as an internal store.

1.6.4.2.2 The auto-trigger level is derived by measuring the positive and negative peaks of the input signal. If the peak-to-peak value exceeds 5.1V or if either peak is outside the range ± 5.1V, the x10 attenuator is automatically switched in. The trigger level is then set to the arithmetic mean of the measured value.

1.6.4.2.3 When operating in the auto-trigger mode, with the x10 attenuator in circuit, the attenuator will be switched out if the peak-to-peak value is less than 4.6V and both peak values are within the range ± 4.6V.

1.6.4.2.4 The trigger levels in use are available at pins mounted on the rear panel of the instrument. The voltage range is ± 5.1V regardless of whether the attenuator is switched in or not, so the voltage should be multiplied by 10 when the x10 attenuator is selected.

1.6.4.3 Input C has a nominal input impedance of 50Ω and is AC-coupled. Protection against excessive signal levels is provided by a fuse mounted in the input socket.

1.6.5 Low-Pass Filter

1.6.5.1 An internal low-pass filter can be introduced to reduce the bandwidth of Channel A to 50 kHz (nominal).

1.6.6 Math Function

1.6.6.1 When the math function is active, the displayed value is:

$$\frac{\text{Measurement Result} - X}{Z}$$

where X and Z are values entered into stores within the instrument by the operator. X is set to 0 and Z to 1 when the instrument is first switched on. By suitable choice of values for X and Z, ratio, offset (null) and percentage-difference displays can be obtained.

1.6.7 Special Functions

1.6.7.1 A number of special functions are available to the operator. These provide test procedures and operating facilities in addition to those available by operation of the front-panel controls. See subsection 3.8 of this manual for further details.

1.6.8 Error Indication

1.6.8.1 When operating the 1992-02M certain errors will result in displayed error codes. See subsection 3.9 of this manual for further details.

1.6.9 External Arming

1.6.9.1 External arming of the start and stop circuits for the measurement interval can be carried out by means of signals connected to a rear-panel mounted socket. Any combination of internal and external arming can be selected by using the appropriate special function. For further details, refer to Subsection 3.8 and 3.11 along with Table 3.12 in this manual.

1.6.10 Display Format

1.6.10.1 The display uses an engineering format, with a nine-digit mantissa and one exponent digit. Overflow of the most significant digits can be used to increase the display resolution.

1.6.11 Hold Feature

1.6.11.1 The hold feature allows readings to be held indefinitely. A new measurement cycle is initiated using the RESET key.

1.6.12 Resolution and Gate Time

1.6.12.1 The counting interval (gate time) in the Total A by B mode is controlled by the time interval between the start and stop signals at the Channel B input. In the Manual Totalize mode, the gate time is determined by successive operations of the HOLD key. In the Frequency A, Frequency C, Period A, Ratio A/B, and Ratio C/B modes, the gate time is determined by the selected display resolution. In Phase mode, the gate time is fixed and the display resolution is determined by the input signal frequency. Details of the relationship between gate time and resolution for each measurement mode are provided in Subsection 3.6 of this manual.

1.6.13 External Frequency Standard Input

1.6.13.1 The 1992-02M may be operated using an external frequency standard. The instrument will operate from the external standard whenever the signal at the EXT STD INPUT socket is of sufficient amplitude. The instrument will automatically revert to internal standard operation if the input from the external standard is removed.

1.6.14 Standby Mode

1.6.14.1 When the instrument is switched to standby, the internal frequency standard continues to operate, but the measuring circuits are disabled.

1.6.15 Initialization

1.6.15.1 When the instrument is first switched on or when it is initialized via the MATE interface, it is set to one of the following two conditions:

	Local Initialization	MATE Initialization
Measurement Function:	Frequency A	Frequency A
Display Resolution:	8 digits	100 ms gate time
Channel A and B Inputs:	Manual trigger AC coupling Positive-slope trigger 1MΩ input impedance Filter disabled Common input disabled	Auto-Trigger DC coupling Positive-slope trigger 1MΩ input impedance Filter disabled Common input disabled
Delay:	Disabled	—
Delay Store:	200 µs	—
Math Function:	Disabled	—
X Store:	0	—
Z Store:	1	—
Hold:	Disabled	Enabled
Special Functions:	Functions 10, 20, 30, 40, 50, 60, and 70 enabled	—

1.6.16 MATE/CIIL Interface

1.6.16.1 The 1992-02M is provided with MATE/CIIL system interface capability. The MATE/CIIL system interface permits selection of all front-panel measurement functions. See Section 4 for system operation.

SECTION 2 INSTALLATION & PREPARATION FOR USE

2.1 INTRODUCTION

2.1.1 This section provides information on unpacking and inspection, reshipment, power connections, storage and temperature, functional checking, and miscellaneous setup procedures for the 1992-02M.

2.2 UNPACKING AND INSPECTION

2.2.1 Before unpacking the counter, check the exterior of the shipping carton for any signs of damage. All irregularities should be noted on the shipping bill. Unpack and remove the instrument carefully from its carton, perserving the factory packaging as much as possible. Inspect the counter for any defect or damage. Notify the carrier immediately if any damage is apparent. Have a qualified person check the instrument for safety before use.

2.3 RESHIPMENT INSTRUCTIONS

2.3.1 Use the original packaging if it is necessary to return the counter to Racal-Dana for calibration and/or servicing. The original shipping carton and the instrument's plastic-foam form will provide the necessary support for safe reshipment. If the original packaging is unavailable, reconstruct it as much as possible. Wrap the counter in plastic; then use plastic spray foam to surround and protect the instrument. Reship in either the original or new, sturdy shipping carton.

2.4 POWER CONNECTIONS

2.4.1 Before operating the counter, verify that the AC voltage selector is correctly set for the local AC supply. The counter operates on 100, 120, 220, or 240 volts, 45 to 450 Hz. The present voltage range can be seen through the small open window in the rear panel to the left of the AC power plug.

2.4.2 Line Voltage Selection

2.4.2.1 The line voltage setting is easily changed by repositioning the small printed circuit card (voltage selector card) which is mounted horizontally in its slot and accessed via the small rear-panel window. Complete the following procedure to change the voltage setting:

a. Remove the AC power cord from the rear panel

b. Remove the keeper bracket with its one screw and washer from the voltage card window. This completely exposes the voltage selector card

c. Remove the voltage selector card via the small window; reposition it in its slot so that the desired line voltage designation is now visible through the window. (Using a small pair of needle-nose pliers in completing this last step is recommended.)

d. Securely replace the keeper bracket using its hardware

e. Connect the power cord to the counter again

2.4.3 Line Fuse

2.4.3.1 Verify that the rating of the line fuse is suitable for the AC voltage range selected. The fuse should be of the 1/4 in x 1 1/4 in, glass cartridge, surge-resistant type. The required rating is:

90V to 127V: 500 mA (Racal-Dana P/N 920204)
123V to 253V: 250 mA (Racal-Dana P/N 920756)

2.4.4 Power Cord and Grounding

2.4.4.1 The front panel and instrument case meet the Type III grounding requirements of MIL-T-28800C, protecting the user from possible injury due to electrical shock.

NOTE:

The 1992-02M is designed to meet IEC Publication 348, "Safety Requirements for Electronic Apparatus for Class I Instruments."

2.4.4.2 A protective ground terminal, forming part of the rear-panel power input socket, is provided. The 1992-02M is supplied with a detachable 3-conductor power cord. Only this cord should be used.

2.4.4.3 Use only AC power outlets having a protective ground for connection to the counter. **DO NOT USE** 2-conductor extension cords or 3-prong to 2-prong adapters that don't provide a protective ground connection. Connection of the power cord to the power outlet must be made in accordance with the following standard color code:

	American	European
Live	Black	Brown
Neutral	White	Blue
Ground (Earth)	Green	Green/Yellow

2.5 STORAGE AND TEMPERATURE

2.5.1 The 1992-02M can be stored at temperatures ranging from -40°C to 75°C at 75% relative humidity without adverse effects to PCBs or components. The counter must be brought within its specified operating range of 0°C to 50°C before power-on.

2.6 FUNCTIONAL CHECK

2.6.1 Introduction

2.6.1.1 The following procedure confirms whether or not the 1992-02M is performing correctly by checking most of the counter's circuitry. The procedure should be conducted when the 1992-02M is first put into service and after shipment to a new location. This procedure does not check that the instrument is operating to published specification. Detailed Performance Verification Procedures (PVPs) are given in Section 6 of this manual.

NOTE:

A 50Ω coaxial test lead, fitted with BNC connectors is required. This lead must be at least 60 cm, but not more than 1m long.

2.6.1.2 Perform the following procedure:

a. Connect the 1992-02M to a suitable AC supply

b. Turn the instrument on. Verify that the instrument's model number appears in the display for approximately two seconds, followed by a number indicating the software version and issue numbers. The instrument should assume the following home state:

1. Display should be 00000000

2. Hz, RESOLUTION, FREQ A, INPUT A ∫, and INPUT B ∫ LEDs should be lit

3. INPUT A and B TRIG LEDs may or may not be lit

c. Press the FUNCTION ↓ key until the CHECK LED lights. Check that the display shows 10.0000000 E6 and that the GATE LED is flashing

d. Verify that the RESOLUTION LED is lit. Press the RESOLUTION↓ key five times, ensuring that the resolution of the display is decreased by one digit each time

e. Press the RESOLUTION ↑ key to increase the display to nine digits

2.6.1.3 If required, the following additional checks may also be performed, using the instrument's special functions.

a. Complete the following key sequence:

[7] [1] [SHIFT] [STORE] [SF] [SHIFT] [SF]

Check that all LEDs, with the exception of TRIG A, TRIG B, GATE and STBY/CHRG flash on and off every two seconds. Verify that REM, ADDR, and SRQ LEDs are illuminated and do not flash

b. Connect the 10 MHz STD OUTPUT socket on the rear panel to the front panel INPUT A connector, using the coaxial test lead

c. Complete the following key sequence:

[7] [7] [SHIFT] [STORE] [SF]

Verify that the display shows *0.******* E0 Hz after about 6 seconds (where * indicates a blanked digit). The x10, 50Ω, DC, FILTER and COM A LEDs for Channel A should light sequentially

d. Disconnect the coaxial lead from the INPUT A connector. The display should show an error number after a few seconds

e. Connect the coaxial lead to the INPUT B connector

f. Complete the following procedure:

[7] [8] [SHIFT] [STORE] [SF]

Check that the display shows *0.******* E0 Hz after about 4 seconds. The x10, 50Ω and DC LEDs for Channel B should light sequentially

g. Disconnect the coaxial lead from the INPUT B connector and the 10 MHz STD OUT connector. The display should show an error number after a few seconds

h. Switch the instrument off

2.7 MISCELLANEOUS SETUP PROCEDURES

2.7.1 Frequency Standard

2.7.1.1 If it is intended to use an external frequency standard, the output of the frequency standard should be connected to the EXT STD INPUT connector on the rear panel of the instrument. The connection should be made using coaxial cable. Switch on the frequency standard and the instrument: check that the EXT STD LED on the front panel of the instrument lights.

2.7.1.2 A 10 MHz signal, derived from the internal frequency standard, is available at the 10 MHz STD OUT connector on the rear panel of the instrument. If this signal is used, the connection should be made using coaxial cable.

2.7.2 External Arming

2.7.2.1 If external arming is to be used, the arming signal should be connected to the EXT ARM INPUT connector on the rear panel.

2.7.3 Trigger Level Output

2.7.3.1 The trigger levels in use on Channels A and B are available via pins on the instrument's rear panel. If required, connection to the pins should be made using a clip-on probe or small alligator clip.

2.8 GPIB PREPARATION FOR USE

2.8.1 Introduction

2.8.1.1 The instrument must be prepared for use in accordance with the instructions given in Subsection 2.4 prior to implementing instructions provided in this subsection.

2.8.2 GPIB Connection

2.8.2.1 Connection to the GPIB is made via a standard IEEE-488 connector, mounted on the rear panel. The pin assignment is given in Table 2.1. An adapter, Racal-Dana P/N 23-3254, to convert the connector to the IEC 625-1 standard is available as an optional accessory.

Table 2.1 - GPIB Connector Pin Assignment

PIN	SIGNAL LINE	PIN	SIGNAL LINE
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	Gnd (6)
7	NRFD	19	Gnd (7)
8	NDAC	20	Gnd (8)
9	IFC	21	Gnd (9)
10	SRQ	22	Gnd (10)
11	ATN	23	Gnd (11)
12	SHIELD	24	Gnd (5 and 71)

2.8.3 Address Setting and Display

2.8.3.1 The interface address is set using five switches, A1 to A5, which are mounted on the rear panel. The permitted address settings, in binary, decimal, and ASCII character form, are given in Table 2.2. The GPIB address set can be displayed, in decimal form, by pressing:

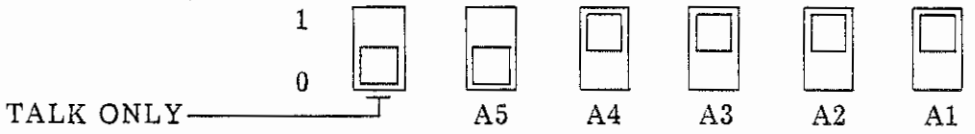
[SHIFT] [RECALL] [RESET]

If the address is changed, this key sequence must be repeated to display the new address. The instrument is returned to the measurement mode by pressing:

[CONTINUE]

2.8.3.2 For addressed operation, the TALK ONLY switch must be in the logic 0 position (down).

Table 2.2 - Address Switch Settings



SWITCH SETTINGS					ADDRESS CODES		
A5	A4	A3	A2	A1	DECIMAL	ASCII LISTEN ADDRESS	ASCII TALK ADDRESS
0	0	0	0	0	0	SP	@
0	0	0	0	1	1	!	A
0	0	0	1	0	2	"	B
0	0	0	1	1	3	#	C
0	0	1	0	0	4	$	D
0	0	1	0	1	5	%	E
0	0	1	1	0	6	&	F
0	0	1	1	1	7	'	G
0	1	0	0	0	8	(	H
0	1	0	0	1	9	)	I
0	1	0	1	0	10	*	J
0	1	0	1	1	11	+	K
0	1	1	0	0	12	,	L
0	1	1	0	1	13	-	M
0	1	1	1	0	14	.	N
0	1	1	1	1	15	/	O
1	0	0	0	0	16	0	P
1	0	0	0	1	17	1	Q
1	0	0	1	0	18	2	R
1	0	0	1	1	19	3	S
1	0	1	0	0	20	4	T
1	0	1	0	1	21	5	U
1	0	1	1	0	22	6	V
1	0	1	1	1	23	7	W
1	1	0	0	0	24	8	X
1	1	0	0	1	25	9	Y
1	1	0	1	0	26	:	Z
1	1	0	1	1	27	;	[
1	1	1	0	0	28	<	\
1	1	1	0	1	29	=	]
1	1	1	1	0	30	>	^

Instrument shipped with one of these four settings

2.8.4 GPIB Check

2.8.4.1 The procedure which follows checks the ability of the instrument to accept, process, and send GPIB messages. The correct functioning of the instrument under local control should be verified before the procedure is attempted.

2.8.4.2 The recommended test equipment is the Hewlett-Packard HP-85 GPIB controller, with the I/O ROM in the drawer. It is assumed that the select code of the controller I/O port is 7. If any other controller is used, the GPIB commands given in the following paragraphs may require modification. The controller should be connected to the GPIB interface of the instrument via a GPIB cable. No connection should be made to the Channel A, B, or C inputs.

2.8.4.3 Successful completion of the GPIB check proves that the instrument's GPIB ithatface is operating correctly. The procedure does not check that all the device-function commands can be executed. However, if the GPIB interface works correctly and the instrument operates correctly under local control, there is a high probability that it will respond to all device-function commands.

2.8.4.4 Switch the instrument on. Check that the REM, ADDR, and SRQ LEDs flash on and off once. If the indicators do not flash, or if they flash continuously, there is a fault on the GPIB board. Verify that the instrument assumes the home state described in Subsection 2.6.1.2.

2.8.4.5 Run the following program to execute the GPIB check:

```
10  DIM  R$[80]

20  C = 7nn (where nn is the number displayed in Subsection 2.8.3.1.

30  OUTPUT C; "IST"

40  OUTPUT C; "STA"

50  ENTER C; R$

60  IF R$[1,1] = "F" THEN GO TO 90

70  PRINT "UNIT PASSES GPIB CHECK"

80  END

90  PRINT "UNIT FAILS GPIB CHECK"

100 PRINT

110 PRINT "ERROR MESSAGE IS", R$

120 GO TO 80
```

3.1 INTRODUCTION

3.1.1 This section contains information for operating the 1992-02M as a bench instrument. It provides Front and Rear Panel Descriptions, Operating Procedures, and Miscellaneous Operating Information.

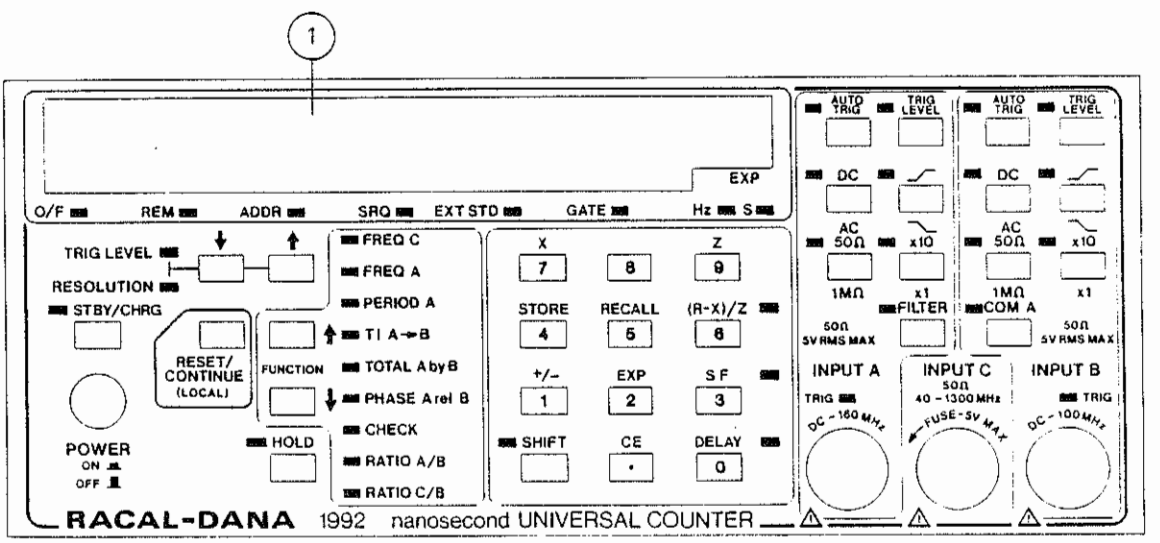
3.1.2 The instrument should be prepared for use in accordance with the instructions given in Section 2. If the instrument is being used for the first time or at a new location, ensure that the setting of the AC voltage selector is correct.

3.2 PANEL DESCRIPTIONS

3.2.1 Front Panel Features

3.2.1.1 Refer to Table 3.1 and the front-panel figures. They show and briefly describe the front-panel controls, indicators, and connectors.

Table 3.1 - Front-Panel Controls, Indicators, and Connectors

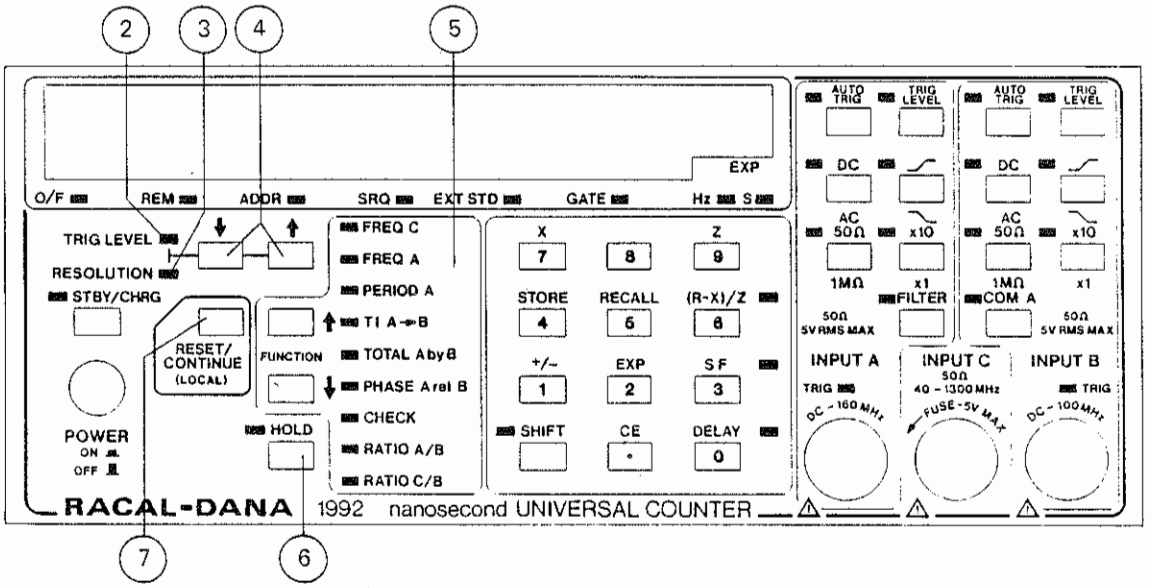


Reference	Item	Function/Description
1	Display	A 7-segment LED digital display. Used to display: - measurement results - numbers for entry into an internal store - numbers recalled from an internal store - error messages The display format uses an engineering format with 9-digit mantissa and 1-digit exponent. The exponent is normally a multiple of three

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
		The exponent digit is blanked and should be assumed to be zero during the following: a. Phase measurement b. Totalize measurement with less than ten digits c. Number entries from the numeric keypad not involving an exponent
	O/F LED	Lights when the readout overflows the ninth digit of the display
	REM LED	Lights when the instrument is operating under remote control
	ADDR LED	Lights when the instrument is acting as a listener or as a talker
	SRQ LED	Lights when the instrument generates a service request
	EXT STD LED	Lights when the instrument is operating from an external frequency standard
	GATE LED	Lights while a measurement cycle is in progress
	Display Units LEDs	The Hz indicator lights for a frequency display. The s indicator lights for a time display. Neither indicator lights for a display of phase angle, ratio, total, trigger level, or a number
(2)	TRIG LEVEL Control LED	Lights when a trigger level is being displayed. The displayed trigger level can be stepped up or down using the ↑ and ↓ keys, or can be changed using the numeric keyboard
(3)	RESOLUTION Control LED	Lights to show that the resolution of the display can be changed by means of the ↑ or ↓ control keys

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)



Reference	Item	Function/Description
4	Step-Up ↑ and Step-Down ↓ Keys	Used to step the display resolution or the displayed value of trigger level up or down
5	FUNCTION Keys (↑↓)	Select in succession the counter's measurement functions. The corresponding FUNCTION LED is lit. Function selection "wraps around" at both ends
6	HOLD Key	Successive operation toggles the instrument in and out of the Hold (single-shot measurement) mode. The LED lights in the Hold mode. Readings are triggered using the RESET key When the instrument is in the Manual Totalize mode (using Special Function 61), successive operation of the HOLD key will start and stop the measurement cycle
7	RESET/CONTINUE (LOCAL) Key	This key has the following three functions: RESET Clears the display and triggers a new measurement cycle when the instrument is in the measurement mode

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)

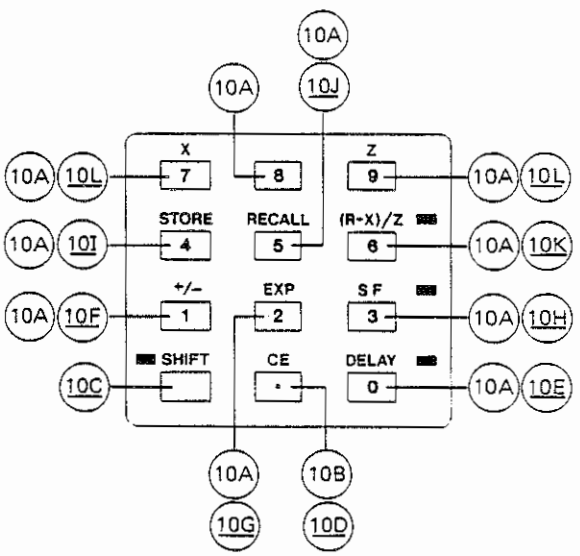
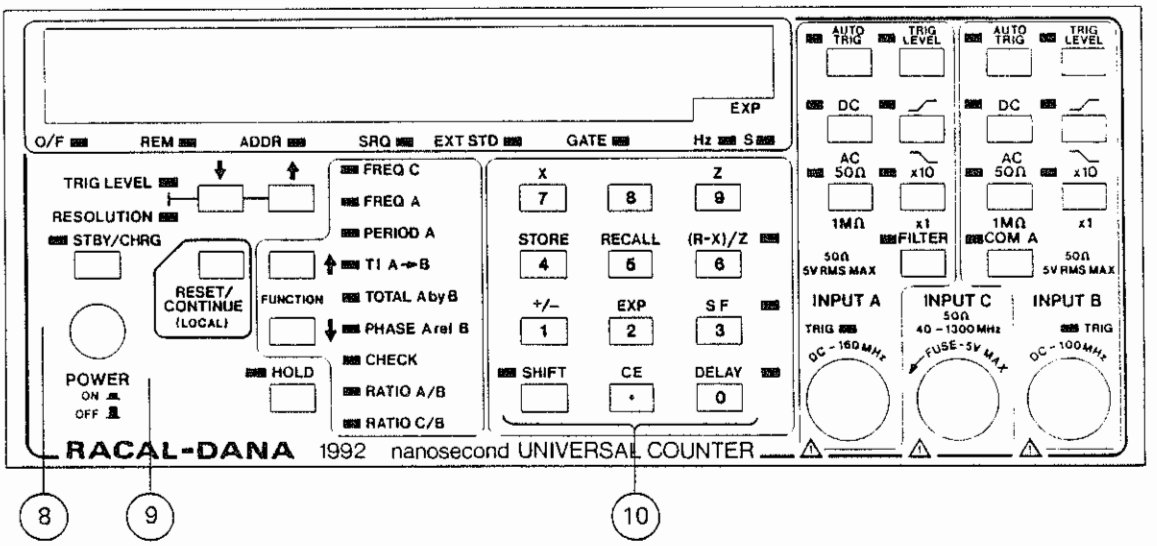
Reference	Item	Function/Description
		CONTINUE Returns the instrument to the measurement mode and triggers a measurement cycle, following the display of a number or constant recalled from store. It can also be used to clear the OP Er display LOCAL Returns the instrument to front-panel control from remote GPIB control, provided local lockout is not set
(8)	STBY/CHRG Key	Successive operation toggles the instrument in and out of the standby state. The LED lights when the instrument is in the standby state. In standby, power is supplied only to internal frequency standard and memories
(9)	POWER (ON/OFF) Button	Controls the AC power to the instrument
(10)	Data Entry Keys/LEDs	Permit data entry and user interface with the 1992-02M other than input signal conditioning and measurement functions
	NOTE: Designators for shifted key functions are underlined	
	Unshifted Key Functions:	
(10A)	Numeric Keys (0-9)	Entry of numbers and constants for math, special functions, time-interval stop delays and trigger levels. When a numeric key is pressed, the measurement in progress is aborted and the display shows the entered number

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)



Reference	Item	Function/Description
10B	Decimal Point (.) Key	Inserts a decimal point during numeric entry
	Shifted Key Functions:	
10C	SHIFT Key/LED	Enables any shifted key function. After pressing a shifted key function (except for STORE and RECALL), counter returns to its unshifted state with the SHIFT LED turning off
10D	CE Key	Clears current display number and entry
10E	DELAY Key/LED	Enables a TI A→B or Totalize A by B stop delay (SHIFT DELAY). Also, stores (<value> SHIFT STORE DELAY), and recalls (SHIFT RECALL DELAY) a stored stop delay
10F	Positive/Negative (+/-) Sign Key	Toggles sign of entered number (mantissa and/or exponent) between positive (no sign displayed) and negative (sign displayed)
10G	EXP Key	Changes the data entry mode so that the next number entered is the exponent

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
10H	SF Key/LED	Enables all selected special functions (SHIFT SF). Also, stores (<NN> SHIFT STORE SF) and recalls (SHIFT RECALL SF) special functions. See Subsection 3.8 for further details
10I	STORE Key	Stores constants for math functions, time-interval delay, and special functions
10J	RECALL Key	Recalls constants for math functions, time-interval delay, and special functions
10K	(R-X)/Z Math Key/LED	Enables selection of Math computation mode
10L	X/Z Keys	Store and recall Math computation constants (X and Z)
11	INPUT A and B Signal Conditioning Keys/LEDs	
11A	AUTO TRIG Keys/LEDs	Toggles to select auto-trigger or manual trigger level. The LED lights when auto-trigger is selected

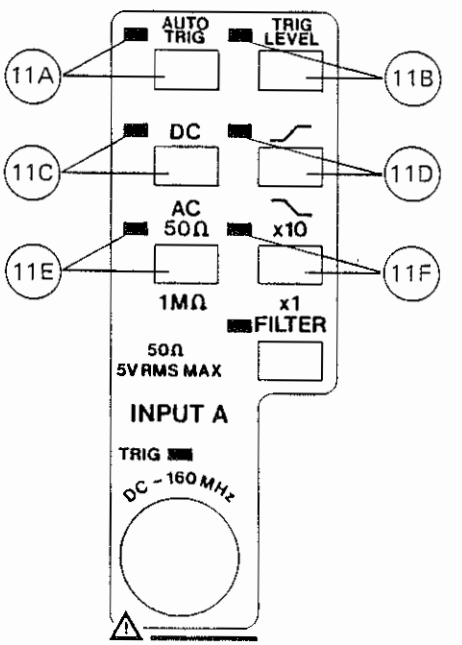
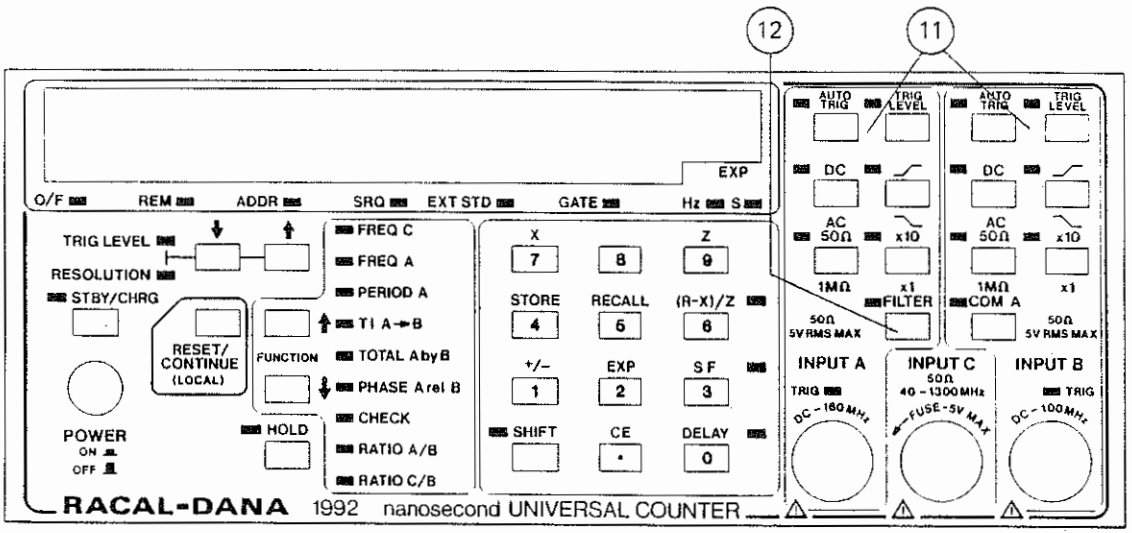


Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)

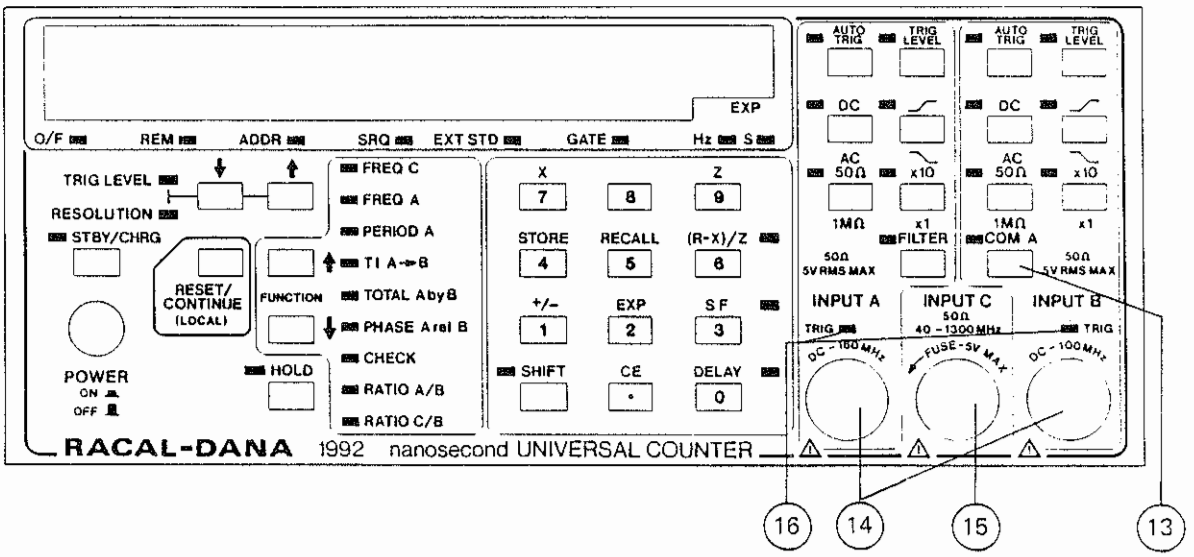


Reference	Item	Function/Description
(11B)	TRIG LEVEL Keys/LEDs	Toggles to display the trigger level in use or to enter a new trigger level. The LED flashes when the trigger level is being displayed. (The trigger level control LED (2) will also light.)
(11C)	DC/AC Keys/LEDs	Toggles to select AC or DC coupling of the input signal. The LED lights when DC coupling is selected
(11D)	⎍/⎏ Keys/LEDs	Toggles to select the positive-going (⎍) or negative-going (⎏) edge of the input waveform for triggering The LED lights when the positive-going edge is selected
(11E)	50Ω /1MΩ Keys/LEDs	Toggles to select 50Ω or 1MΩ input impedance. The LED lights when 50Ω is selected
(11F)	x10/x1 Keys/LEDs	Toggles to select attenuation of the input signal. With x10 selected, the input is attenuated by a factor of 10. The LED lights when x10 is selected
(12)	FILTER Key/LED	Toggles to enable or disable the Channel A's input filter. LED lights when the filter is enabled

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
(13)	COM A Key/LED	Toggles to connect or disconnect the signal at Channel A's input into both Channels A and B (parallel COMmon configuration) LED lights when the COM mode is selected In COM mode, Channel A's AUTO TRIG key controls both Channels A and B. Channel B's AUTO TRIG key is rendered inoperative. Channel B's AUTO TRIG LED follows the lit/unlit state of Channel A's LED Both Channels A and B adopt the same trigger level with auto-trigger level selected. Different trigger levels can be set in the two channels , however, when manual trigger level is selected Channel A's 50Ω/1MΩ, x10/x1 and DC/AC keys control both channels. Channel B's x10/x1 and DC/AC LEDs follow the lit/unlit state of Channel A's LEDs. Channel B's 50Ω/1MΩ LED continues to show the impedance of Channel B's input
(14)	INPUT(s) A and B	BNC connectors for INPUT(s) A and B. INPUT A (DC to 160 MHz) is used for all functions except Frequency C. INPUT B (DC to 100 MHz) is used with INPUT A for Time Interval, Ratio A/B, Totalize, and Phase measurement. INPUT B is used with INPUT C for Ratio C/B. Special Function 21 internally exchanges INPUTs A and B (providing, e.g., PERIOD B, etc. measurement capability)

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)



Reference	Item	Function/Description
(15)	INPUT C	BNC connector for high-frequency INPUT C (40 MHz - 1.3 GHz). INPUT C is used with INPUT B for Ratio C/B. Special Function 21 provides Ratio C/A capability. Protection against excessive signal levels (> 5V rms) is provided by a fuse mounted in the input socket
(16)	TRIG LEDs/Inputs A and B	Tri-state LEDs indicating the counter's trigger status: a. **LED On** - trigger level too low or input signal level held in a high state b. **LED Flashing** - channel being triggered c. **LED Off** - trigger level too high or input signal level held in a low state

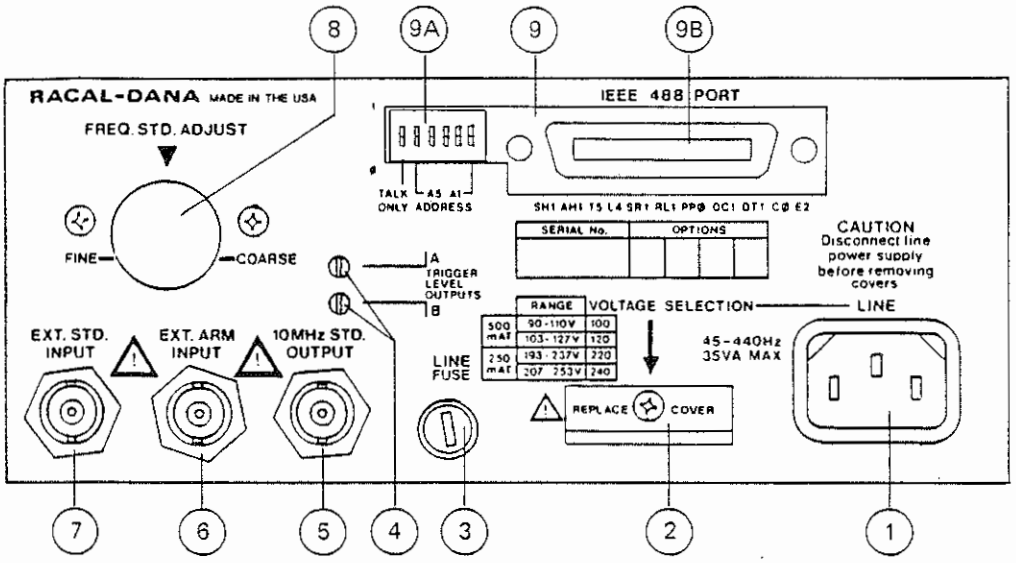
3.2.2 Rear Panel Features

3.2.2.1 Refer to Table 3.2 and figure at top. They show and briefly describe the rear-panel controls and connectors.

Table 3.2 - Rear-Panel Controls and Connectors

Reference	Item	Function/Description
(1)	AC Power Input Socket	Standard connector for the AC power supply. A RFI filter is incorporated on the instrument motherboard
(2)	VOLTAGE SELECTION Window	Line voltage selection is changed by repositioning a small printed circuit card inside the instrument. The selected voltage can be viewed through the small open window. See Subsection 2.4.2 for line voltage selection procedure
(3)	LINE FUSE	A 1/4 in x 1-1/4 in glass cartridge Slow-Blow fuse. Line fuse ratings for available line voltages are shown on the rear panel to the right of the fuse receptacle. See also Subsection 2.4.3 in this manual
(4)	TRIGGER LEVEL OUTPUTS (A, B)	Outputs for Inputs A and B trigger levels. Voltage range at both output pins is ± 5.1V, regardless of attenuation
	NOTE: Connectors (5) through (7) are BNCs	
(5)	10 MHz STD. OUTPUT Connector	Output for 10 MHz signal from the internal reference standard
(6)	EXT. ARM INPUT Connector	Input for accepting external arming/gating control signals
(7)	EXT. STD. INPUT Connector	Input for connecting an external frequency standard. The instrument will operate from the external frequency standard whenever a signal of suitable frequency and amplitude is applied. The frequency required is 10 MHz
(8)	FREQ. STD. ADJUST	Aperture providing access for adjusting the internal frequency standard

Table 3.2 - Rear-Panel Controls and Connectors (Cont'd)



Reference	Item	Function/Description
(9)	GPIB Option	
(9A)	GPIB Address Switches	Switches A1 to A5 define the listen and talk addresses for GPIB operation in the addressed mode. The 2-digit GPIB address can be recalled to display using key sequence SHIFT RECALL RESET
(9B)	GPIB Connector	An IEEE-488-1978 standard connector

3.3 OPERATING PROCEDURES

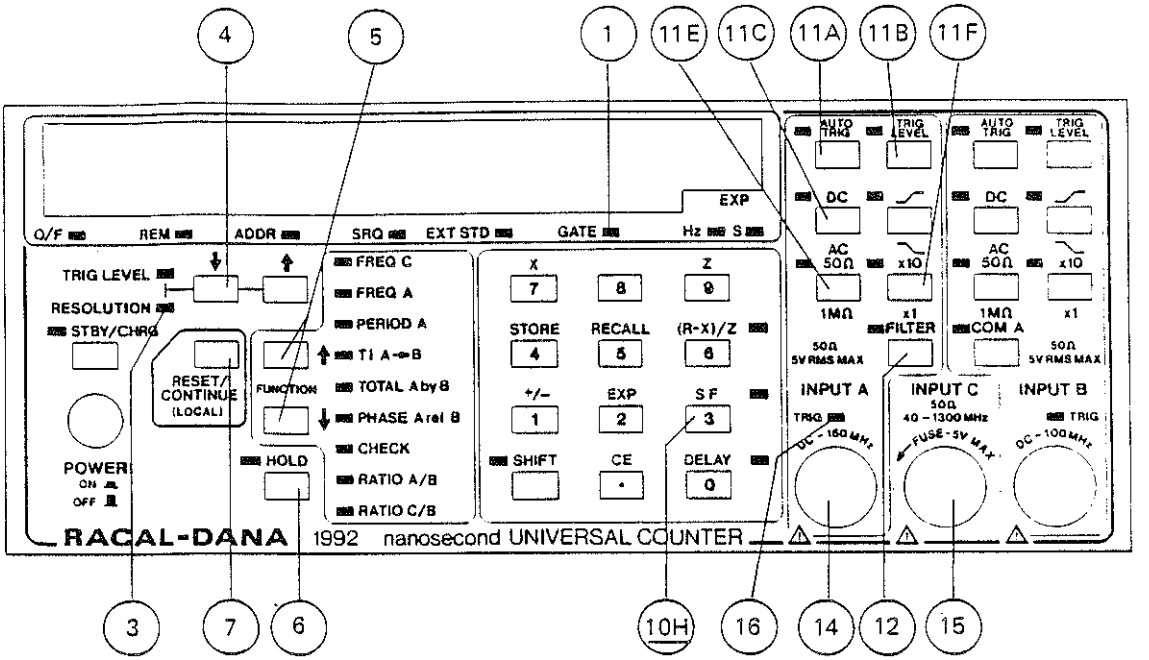
3.3.1 Measurement Functions

3.3.1.1 Tables 3.3 - 3.9 with figures describe the basic bench functions of the 1992-02M.

NOTE:

Review as required Table 3.1, References (14) and (15), for use of Inputs A, B, and C, including Special Function 21 permitting interchange of Inputs A and B. See also Subsection 3.8. and Table 3.10 for special functions.

Table 3.3 - Frequency Measurement



1. Turn power on.

2. Select FREQ A or FREQ C using FUNCTION keys (5).

3. If FREQ A is selected, set the AC/DC coupling (11C), input impedance (11E), and attenuator (11F) as required.

CAUTION

Ensure that the measurement signal does not exceed the damage levels specified in Table 1.1 of this manual.

4. Connect the measurement signal to INPUT A (DC to 160 MHz) (14) or INPUT C (40 MHz to 1.3 GHz) (15).

5. If FREQ A is selected, select AUTO-TRIG (11A), or set the manual trigger level (11B) to the required value. Check that Input A TRIG LED (16) flashes.

6. Select the required display resolution (3)(4).

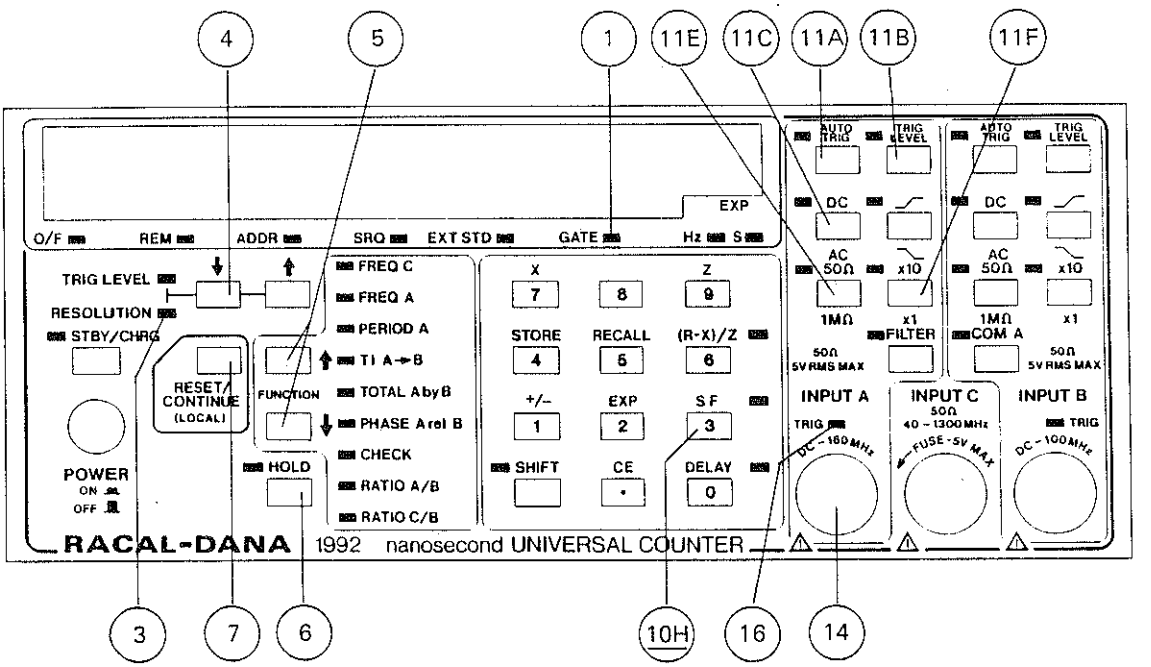
7. If a frequency below 50 kHz is to be measured in the presence of noise, select the filter (12).

8. If external arming is to be used, connect the arming signal and enter the required special function number. Enable the special functions (10H). Refer to Subsection 3.8. for special function numbers and procedures.

9. Verify that the GATE LED (1) flashes on during gating.

10. If single-shot operation is required, select HOLD (6) and press the RESET key (7) to trigger each new measurement.

Table 3.4 - Period Measurement



1. Turn power on.

2. Select PERIOD A using FUNCTION keys (5)

3. Set the AC/DC coupling (11C), input impedance (11E), and attenuator (11F) for Channel A, as required.

CAUTION

Ensure that the measurement signal does not exceed the damage level specified in Table 1.1. of this manual.

4. Connect the measurement signal to INPUT A (14).

5. Select AUTO-TRIG (11A) or set the manual trigger level (11B) to the required value. Check that Input A TRIG LED (16) flashes.

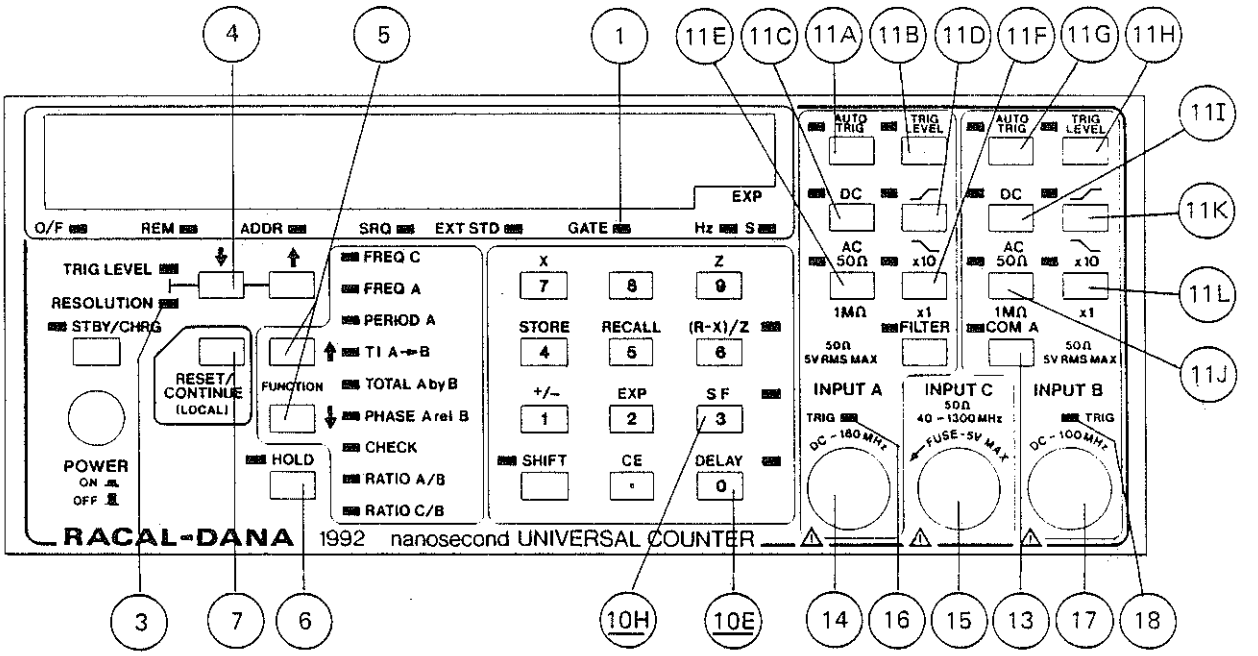
6. Select the required display resolution (3) (4).

7. If external arming is to be used, connect the arming signal and enter the required special function number. Enable the special functions (10H). Refer to Subsection 3.8 for special function numbers and procedures.

8. Verify that the GATE LED (1) flashes on during gating.

9. If single-shot operation is required, select HOLD (6) and press the RESET key (7) to trigger each new measurement.

Table 3.5 - Time Interval Measurement



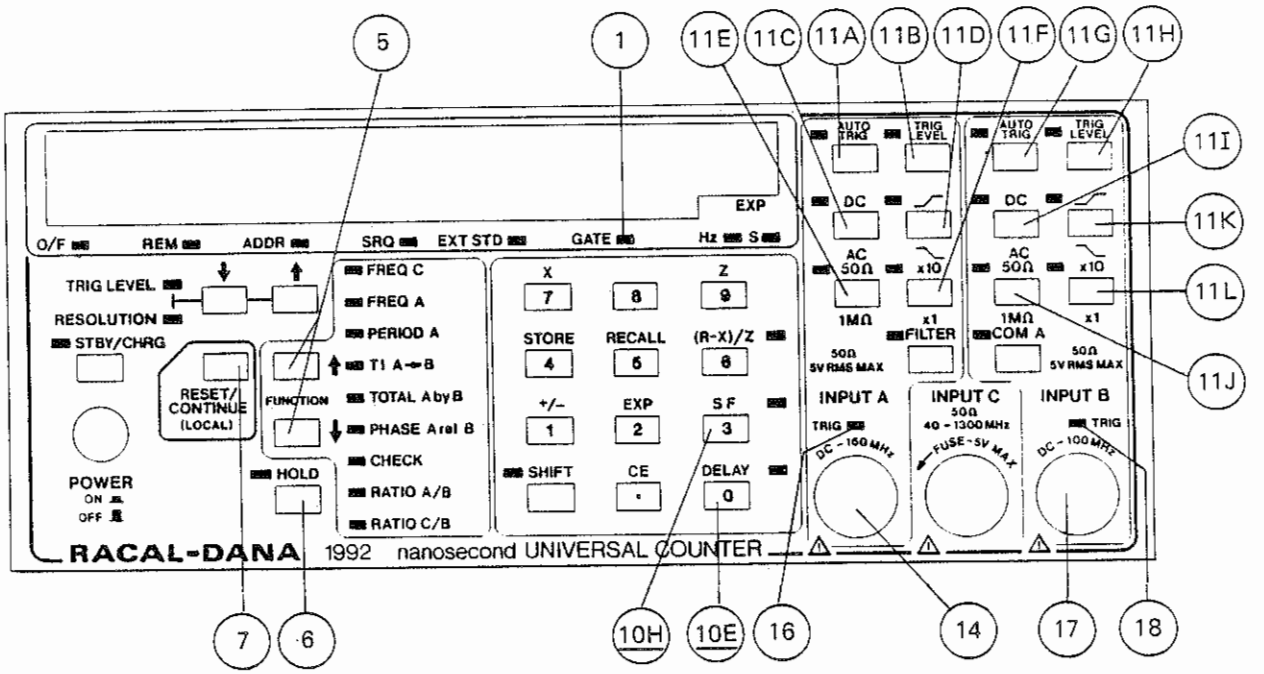
1. Turn power on.
2. Select T.I. A→B using FUNCTION keys (5).
3. Set the AC/DC coupling (11C) / (11I), input impedance (11E) / (11J), attenuator (11F) / (11L), and slope (11D) / (11K), as required. If the start and stop signals are from the **same source,** select COM A (13).

CAUTION

Ensure that the input signals do not exceed the damage levels specified in Table 1.1 of this manual.

4. Connect the start signal to INPUT A (14). If a separate source for the stop signal is used, connect the stop signal to INPUT B (17) and set the associated input controls as needed.
5. Select AUTO-TRIG (11A) / (11G) or set the manual trigger levels (11B) / (11H) to the required values. Check that Inputs A and B TRIG LEDs (16) and (18) flash, respectively.
6. Select the required display resolution (3) (4).
7. If internal delayed arming of the stop circuit is required, enter the delay into memory and enable the delay (10E).
8. If external arming is to be used, connect the the arming signal and enter the required special function number. Enable the special functions (10H). Refer to Subsection 3.8 for special function numbers and procedures.
9. Verify that the GATE LED (1) flashes on during gating.
10. If single-shot operation is required, select HOLD (6) and press the RESET key (7) to trigger each new measurement.

Table 3.6 - Total A by B Measurement



1. Turn power on.

2. Select TOTAL A by B using FUNCTION keys (5).

3. Set the AC/DC coupling (11C) / (11I), input impedance (11E) / (11J), attenuator (11F) / (11L), and slope (11D) / (11K) as required for both Channels A and B.

NOTE:

The INPUT A slope key selects the slope of the events which are counted. The gate time, however, starts on the slope of the Channel B signal selected by the INPUT B slope key and stops on the opposite slope.

CAUTION

Ensure that the signal levels do not exceed the damage levels specified in Table 1.1 of this manual.

4. Connect the signal to be totalized to INPUT A (14) and the control signal to INPUT B (17).

5. Select AUTO-TRIG (11A) / (11G) or set the manual trigger levels (11B) / (11H) to the required values. Check that Inputs A and B TRIG LEDS (16) and (18) flash, respectively.

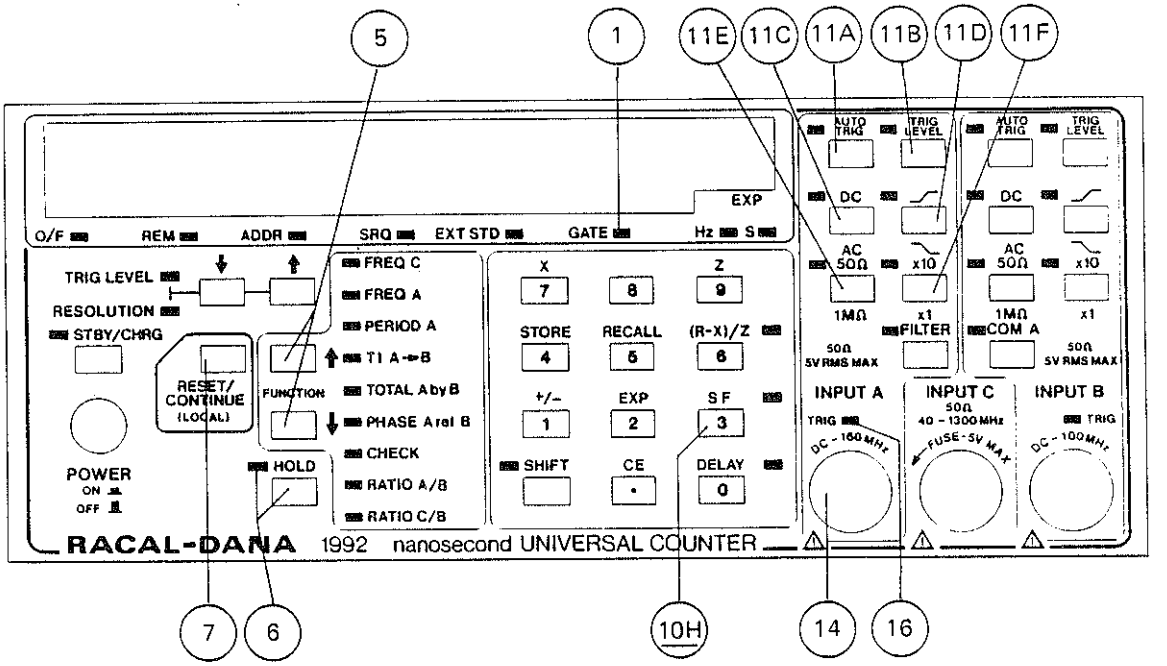
6. If internal delayed arming of the stop circuit is to be used, enter the delay into memory and enable the delay (10E).

7. If external arming is to be used, connect the arming signal and enter the required special function number. Enable special functions (10H). Refer to Subsection 3.8 for special function numbers and procedures.

8. Verify that the GATE LED (1) flashes on when Channel B signal is either high or low.

9. If single-shot operation is required, select HOLD (6) and press the RESET key (7) to trigger each new measurement.

Table 3.7 - Manual Totalize Measurement



1. Turn power on.

2. Select TOTAL A by B using FUNCTION keys (5).

3. Set the AC/DC coupling (11C), input impedance (11E), attenuator (11F), and slope (11D) of Channel A as required.

4. Enter Special Function number 61 and enable special functions (10H). The HOLD LED (6) will light.

CAUTION

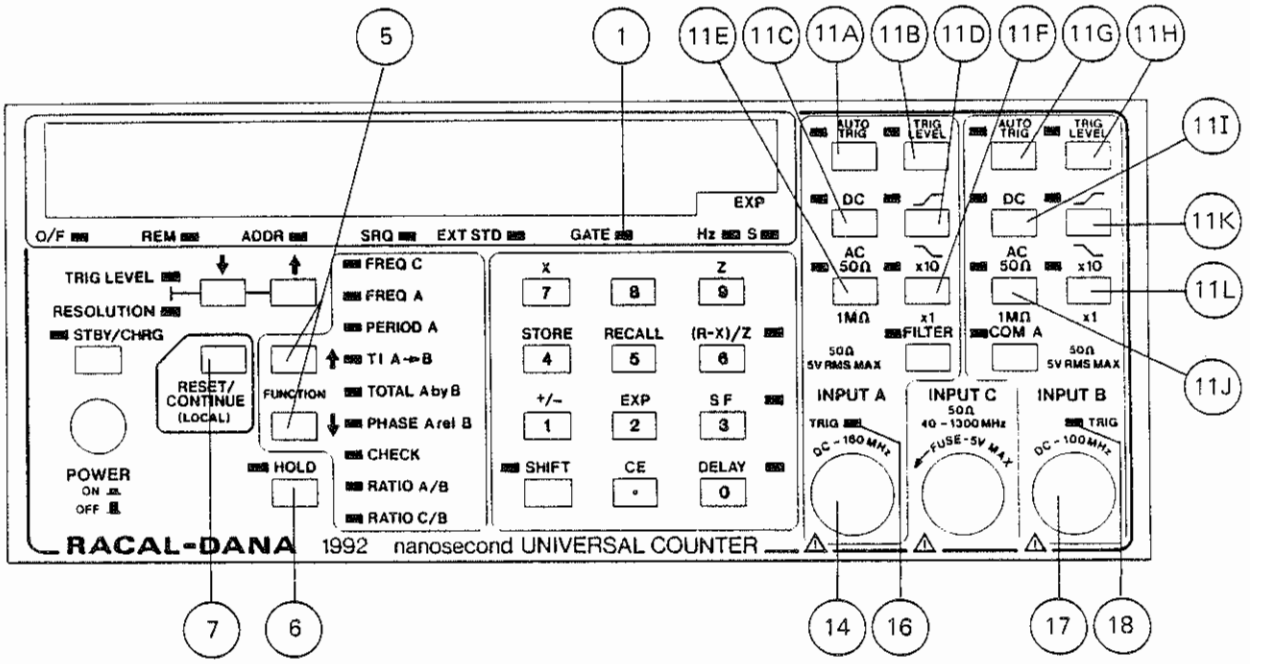
Ensure that the input signal level does not exceed the damage levels specified in Table 1.1 of this manual.

5. Connect the signal to be totalized to INPUT A (14).

6. Select AUTO-TRIG (11A) or set the manual trigger level (11B) to the required value. Check that Input A TRIG LED (16) flashes.

7. Start and stop a measurement using the HOLD key (6). The HOLD LED will turn off and the GATE LED (1) will light during gating. The displayed result is cumulative over successive measurement cycles. If required, use the RESET key (7) to clear the display after a measurement cycle.

Table 3.8 - Phase A rel B Measurement



1. Turn power on.

2. Select PHASE A rel B using FUNCTION keys (5).

3. Set the AC/DC coupling (11C) / (11I), input impedance (11E) / (11J), attenuator (11F) / (11L), and slope (11D) / (11K) as required for INPUTs A and B (14) and (17), respectively . Selected slopes for input signals for Channels A and B should be the same.

CAUTION

Ensure that the input signals do not exceed the damage levels specified in Table 1.1 of this manual.

4. Connect the signals to be compared to INPUT A and INPUT B (14) and (17).

NOTE:

For maximum accuracy, connect the larger and cleaner signal to INPUT A.

5. Select AUTO-TRIG (11A) / (11G) or set the manual trigger levels (11B) / (11H) to the required values. Check that Inputs A and B TRIG LEDs (16) and (18) flash, respectively.

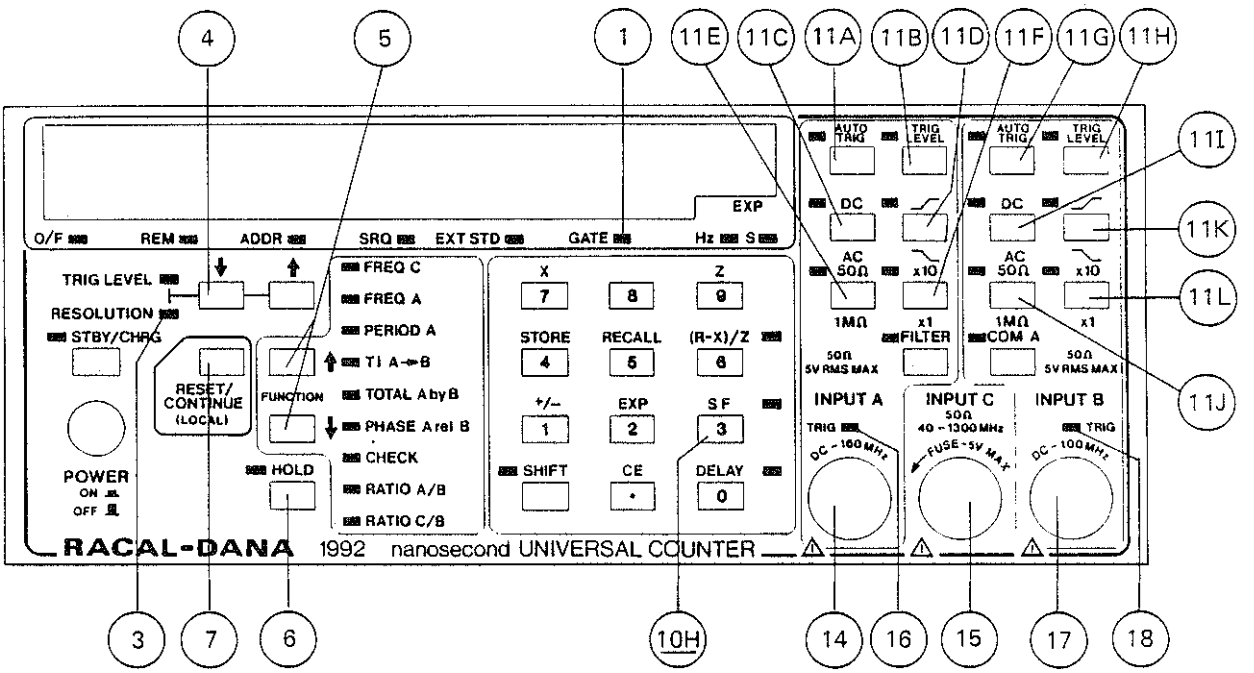
6. Verify that the GATE LED (1) flashes on during gating.

7. If single-shot operation is required, select HOLD (6) and press the RESET key (7) to trigger each new measurement.

NOTE:

A phase measurement is always positive, representing the angle by which Input A's signal leads that of Input B. The signals for phase measurement must be continuous and have the same frequency.

Table 3.9 - Ratio A/B and C/B Measurements



1. Turn power on.

2. Select RATIO A/B or RATIO C/B using FUNCTION keys (5).

3. Set the AC/DC coupling (11C) / (11I), input impedance (11E) / (11J), attenuator (11F) / (11L), and slope (11D) / (11K), as required, for INPUTs A (14) and B (17) and INPUT C (15).

CAUTION

Ensure that the input signals do not exceed the damage levels specified in Table 1.1 of this manual.

4. Connect one of the signals to INPUT B (17) and the other to INPUT A (14) or C (15). The lower frequency signal should be connected to INPUT B (14).

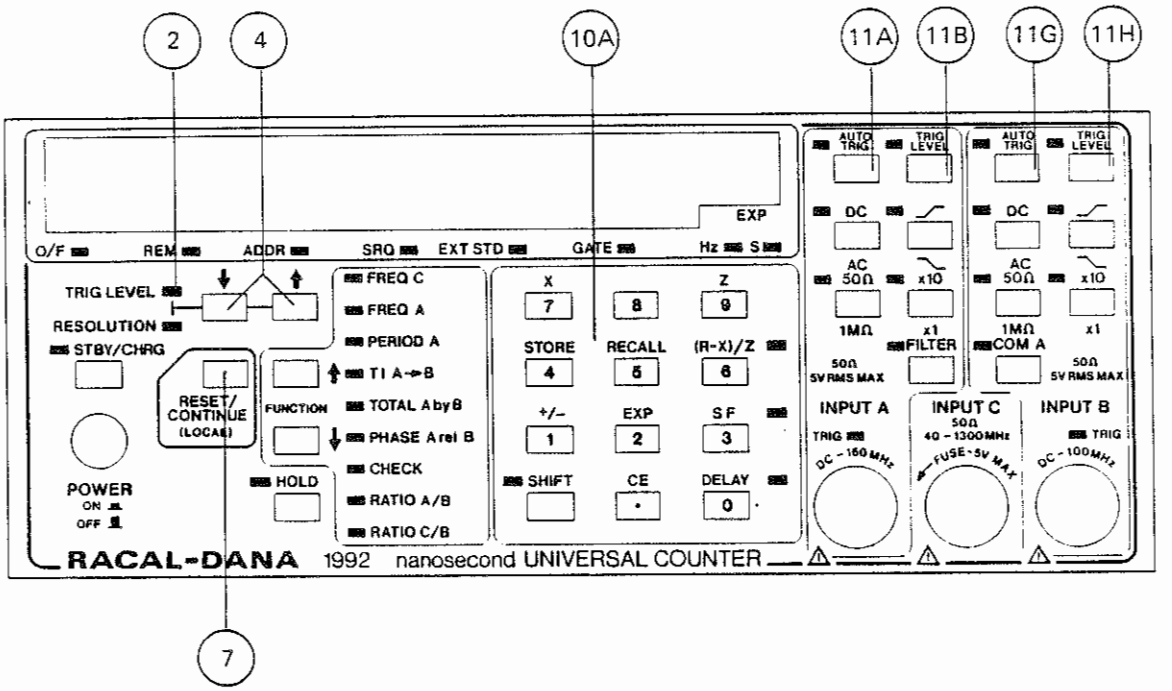
5. Select AUTO-TRIG (11A) / (11G) or set the manual trigger levels (11B) / (11H) to the required values. Check that Inputs A and B TRIG LEDs (16) and (18) flash, respectively.

6. Select the required display resolution (3) (4).

7. If external arming is to be used, connect the the arming signal and enter the required special function number. Enable the special functions (10H). Refer to Subsection 3.8 for special function numbers and procedures.

8. Verify that the GATE LED (1) flashes on during gating.

9. If single-shot operation is required, select HOLD (6) and press the RESET key (7).



3.4 TRIGGER LEVEL

3.4.1 Trigger Level Modes

3.4.1.1 The trigger level may be set by the operator (manual trigger level) or determined automatically by the instrument (auto-trigger level). The auto-trigger level is the arithmetic mean of the positive and negative-peak values of the input signal. The two modes are enabled alternately by successive operations of the AUTO TRIG key (11A) / (11G). The LED lights when the auto-trigger mode is selected.

3.4.2 Displaying and Setting the Manual Trigger Level

3.4.2.1 Perform the following procedure:

a. Select the manual trigger mode using the AUTO TRIG key (11A) / (11G)

b. Display the trigger level by pressing the TRIG LEVEL key (11B) / (11H). The associated LED will flash and the trigger level control LED (2) will light.

c. To change the trigger level:

1. Enter the required value, using the numeric keypad (10A)

NOTE:

Up to this point, the instrument can be returned to the measurement mode with the trigger level unchanged by pressing the CONTINUE key (7)

or

2. Using the step up ↑ or step down ↓ control key (4). The desired trigger level can be entered in 20 mV steps

d. Return the instrument to the measurement mode by pressing the TRIG LEVEL key (11B) / (11H). The TRIG LEVEL LED and the trigger level control LED (2) will extinguish

NOTE:

There is only one trigger level store for each channel. Use of the auto-trigger mode will result in the manual trigger level being overwritten.

3.4.3 Displaying the Auto-Trigger Level

3.4.3.1 Perform the following procedure:

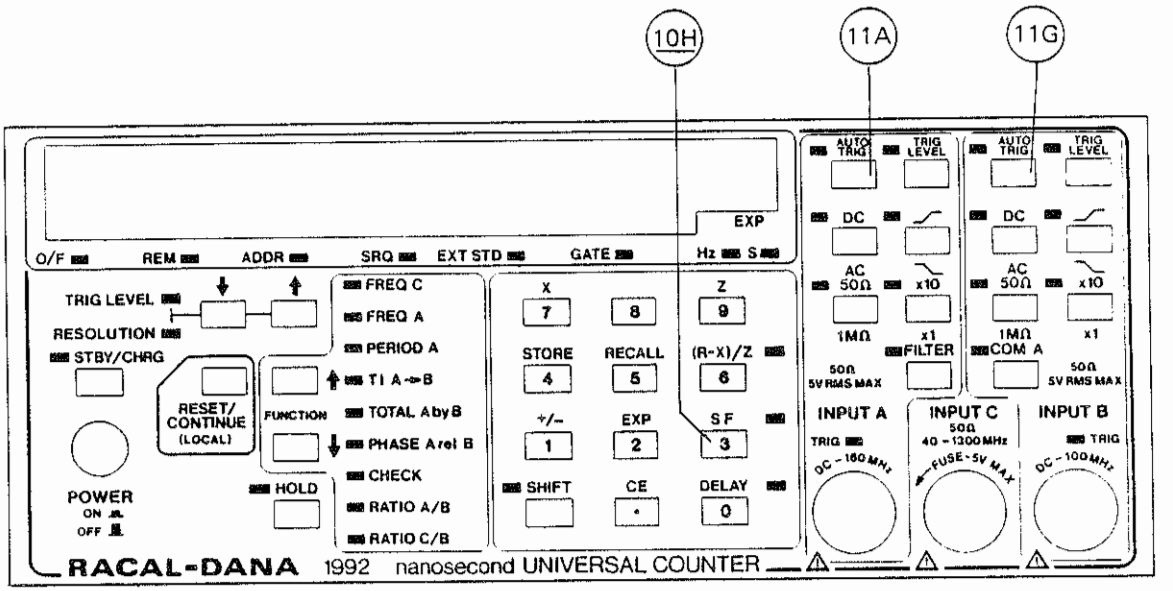
a. Select the auto-trigger mode, using the AUTO TRIG key (11A) / (11G)

b. Display the auto-trigger level by pressing the TRIG LEVEL key (11B) / (11H). The associated LED will flash and the trigger level control LED (2) will light

NOTE:

Any attempt to make a numeric entry while the auto-trigger level is being displayed will cause the OP Er (Operator Error) message to be displayed.

c. Return the instrument to the measurement mode by pressing the TRIG LEVEL key (11B) / (11H) or the CONTINUE key (7). The TRIG LEVEL LED and the trigger level control LED (2) will extinguish



3.4.4 Single-Shot Auto-Trigger Level

3.4.4.1 The auto-trigger level is normally measured continuously and varies if the peak levels of the signal change. A single-shot measurement of auto-trigger level can be made using Special Function 31. This value remains stored as a manual trigger level until:

a. Another single-shot measurement is made, or

b. A new manual trigger level is entered

3.4.4.2 Complete the following to make a single-shot measurement of auto-trigger level:

a. Enter Special Function number 31 into the special function register (10H)

b. Enable the special functions (10H)

c. Select AUTO TRIG (11A) / (11G). The associated LED lights while the level is calculated and stored, and then extinguishes

3.4.4.3 Further single-shot measurements are made by selecting AUTO TRIG (11A) / (11G) with Special Function 31 active.

3.4.5 Automatic Attenuation Setting

3.4.5.1 When operating in the auto-trigger mode, automatic switching of the x10 attenuator occurs as follows:

a. The attenuator is switched in if the peak-to-peak value of the measured signal exceeds 5.1V or if either peak is outside the ±5.1V range

b. The attenuator is switched out if the peak-to-peak value of the measured signal is less than 4.6V and both peaks are within the ±4.6V range

3.5 DISPLAY RESOLUTION

3.5.1 General Information

3.5.1.1 For all measurement functions except TOTAL A by B, the resolution refers to the number of zeros displayed when no signal is applied at the input. The resolution can be set to display 3 to 10 digits. (For a resolution of 10, the most significant digit overflows the display.) A 10% overrange of the display is permitted without a change of range. Because of this, an additional digit with a value of 1 may appear at the more significant end of the display when measurements are made.

3.5.1.2 With some measurement functions, the number of digits appearing may be less than the selected resolution to ensure they are rounded to meaningful values.

3.5.1.3 When ratio measurements are made, no more than eight digits are displayed, regardless of the resolution selected.

3.5.1.4 For the TOTAL A by B, the display shows the true total of events counted from 1 to 999 999 999. For higher totals, the exponent is used.

3.5.1.5 For the PHASE A rel B, up to four digits may be displayed for frequencies up to 1 MHz and up to three digits for higher frequencies. Leading zeros are suppressed. For frequencies above 10 MHz, the resolution of the display is 10^{o}, and a place-holding zero is displayed as the least-significant digit.

3.5.2 Setting the Display Resolution

3.5.2.1 Whenever the resolution control LED is lit, the resolution can be changed using the step-up ↑ and step-down ↓ keys. To step up from nine to ten digits, hold the step-up key down for approximately two seconds.

3.5.3 Resolution with External Stop Circuit Arming

3.5.3.1 When external arming of the stop circuit is used, the minimum display resolution is governed by the arming period as shown in Table 3.10.

Table 3.10 - Resolution with External Arming

Arming Period	Minimum Resolution
Less than 100 µs	4
100 µs to 1 ms	5
1 ms to 10 ms	6
10 ms to 100 ms	7
100 ms to 1s	8
1s to 10s	9

3.6 GATE TIME

3.6.1 For frequency, period, and ratio measurements, the gate time is related to the selected resolution selected as shown in Table 3.11.

Table 3.11 - Resolution and Gate Time

Resolution	Gate Time
10 (9 digits + overflow)	10s
9	1s
8	100 ms (see NOTE 2)
7	10 ms
6	1 ms
5	1 ms
4	1 ms (see NOTE 3)
3	1 ms

NOTE 1:

The gate times shown in the above table are nominal. Due to the use of the recipromatic counting technique, the gate time may be extended by:

a. Up to one period of the input signal on FREQ B and RATIO A/B

b. Up to two periods of the input signal on FREQ A and PERIOD A

c. Up to 64 periods of the input signal on FREQ C and RATIO C/B

NOTE 2:

At power-on, a resolution of 8 is selected.

NOTE 3:

Measurements are averaged when resolutions of 3, 4, or 5 are selected.

3.6.2 For PHASE A rel B, the gate time depends upon the signal frequency. The gate time is approximately 25 ms for frequencies above 200 Hz, but is increased at lower frequencies.

3.7 STOP CIRCUIT DELAY (HOLD OFF)

3.7.1 Use of the Delay

3.7.1.1 The stop circuit can be delayed when T.I. A→B or TOTAL A by B is selected. The required delay is entered into an internal store by the operator. The delay function can then be enabled and disabled as required. At power-up, the delay is set to 204.8 μs (minimum delay).

3.7.1.2 The delay can be used to prevent the stop circuit from being triggered prematurely by spurious signals such as those resulting from relay contact bounce. The principle of stop circuit delay is shown in Figure 3.1.

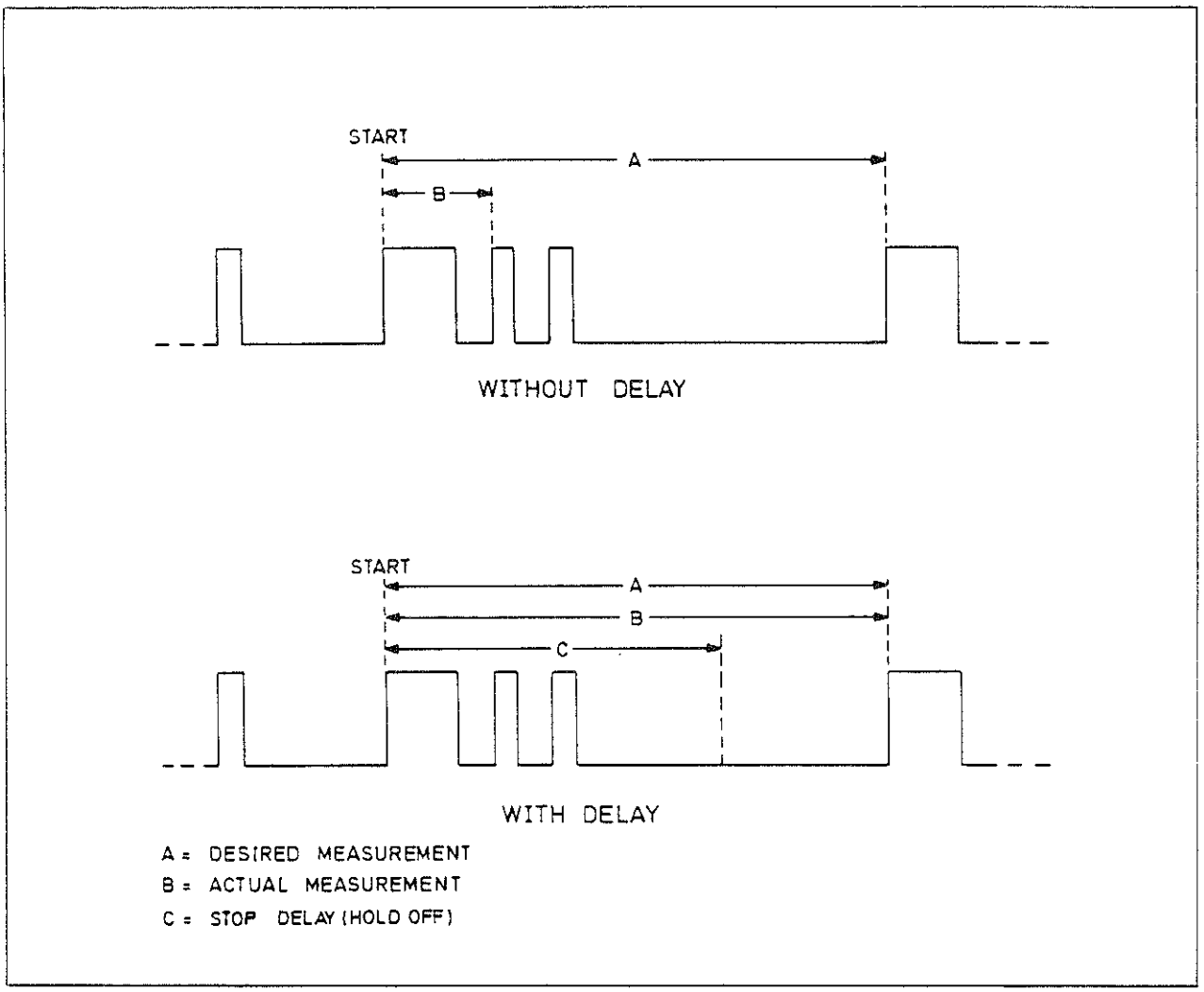


Figure 3.1 - Use of Stop Circuit Delay

3.7.2 Displaying the Delay

3.7.2.1 The value of the delay being stored can be displayed by pressing

[SHIFT] [RECALL] [DELAY]

3.7.3 Changing the Delay

3.7.3.1 A new delay value is entered into its store by using the numeric keypad. Employ either direct decimal or exponential format. For example, a delay of 305 μs may be entered using one of the following key sequences:

[.] [0] [0] [0] [3] [0] [5] [SHIFT] [STORE] [DELAY]

or [3] [0] [5] [SHIFT] [EXP] [6] [SHIFT] [+/-] [SHIFT] [STORE] [DELAY]

The instrument returns to the measurement mode automatically once the new delay value is stored.

3.7.3.2 The value of the delay entered is rounded to the nearest 25.6 μs before it is stored. The permitted range of delay is from 204.8 μs to 800 ms. Attempted entry of an out-of-range value will result in the display of OP Er. The number in the delay store is retained when the instrument is switched to standby.

3.7.4 Enabling and Disabling the Delay

3.7.4.1 The stop delay is enabled and disabled by means of the sequence

[SHIFT] [DELAY]

The DELAY LED lights when the delay is enabled.

3.8 SPECIAL FUNCTIONS

3.8.1 Special Function Numbering

3.8.1.1 The special functions provided for operator use are listed in Table 3.12. Each special function is defined by a two-digit number.

3.8.2 Special Function Register

3.8.2.1 One special function from each decade is entered into a special function register. Only the second digit is stored: the decade is indicated by the position of the digit in the register. The default state is with 0 entered in each position. The contents of the register can be displayed by pressing:

[SHIFT] [RECALL] [SF]

A typical display is illustrated in Figure 3.2.

Table 3.12 - Special Functions

Function Number	Function			
		Start	Stop	
10	Arming	Internal	Internal	
11		External +ve	Internal	
12		External -ve	Internal	
13		Internal	External +ve	
14		Internal	External -ve	
15		External +ve	External +ve	
16		External +ve	External -ve	
17		External -ve	External +ve	
18		External -ve	External -ve	
20	Normal Operation			
21	Channel A and B interchanged (see NOTE 1)			
30	Continuous measurement of auto-trigger level			
31	Single-shot measurement of auto-trigger level			
40	Select elapsed time between displayed measurement cycles	150 ms	between displays	See NOTE 2
41		0	between displays	
42		1s	between displays	
43		10s	between displays	
44		300s	between displays	
50	Value displayed by operation of TRIG LEVEL	Trigger level		
51		Signal positive peak		
52		Signal negative peak		
60	Measurement made with TOTAL A by B selected	Normal TOTAL A by B		
61		Manual Totalize		
70	Function with CHECK selected	10 MHz check		
71		LED check		
72-76	Reserved for diagnostic testing			
77	Channel A relay check			
78	Channel B relay check			

NOTE 1:

Special Function 21 permits FREQ B, PERIOD B, T.I. B→A, TOTAL B by A, and Phase B rel A. For these functions:

a. FREQ B is specified to 100 MHz only
b. PERIOD B is specified down to 10 ns
c. TOTAL B by A operates for one complete cycle of the Channel A signal. The stop circuit delay is available on Channel A

NOTE 2:

Special Functions 40, 42, 43, and 44 are only available when in local control.

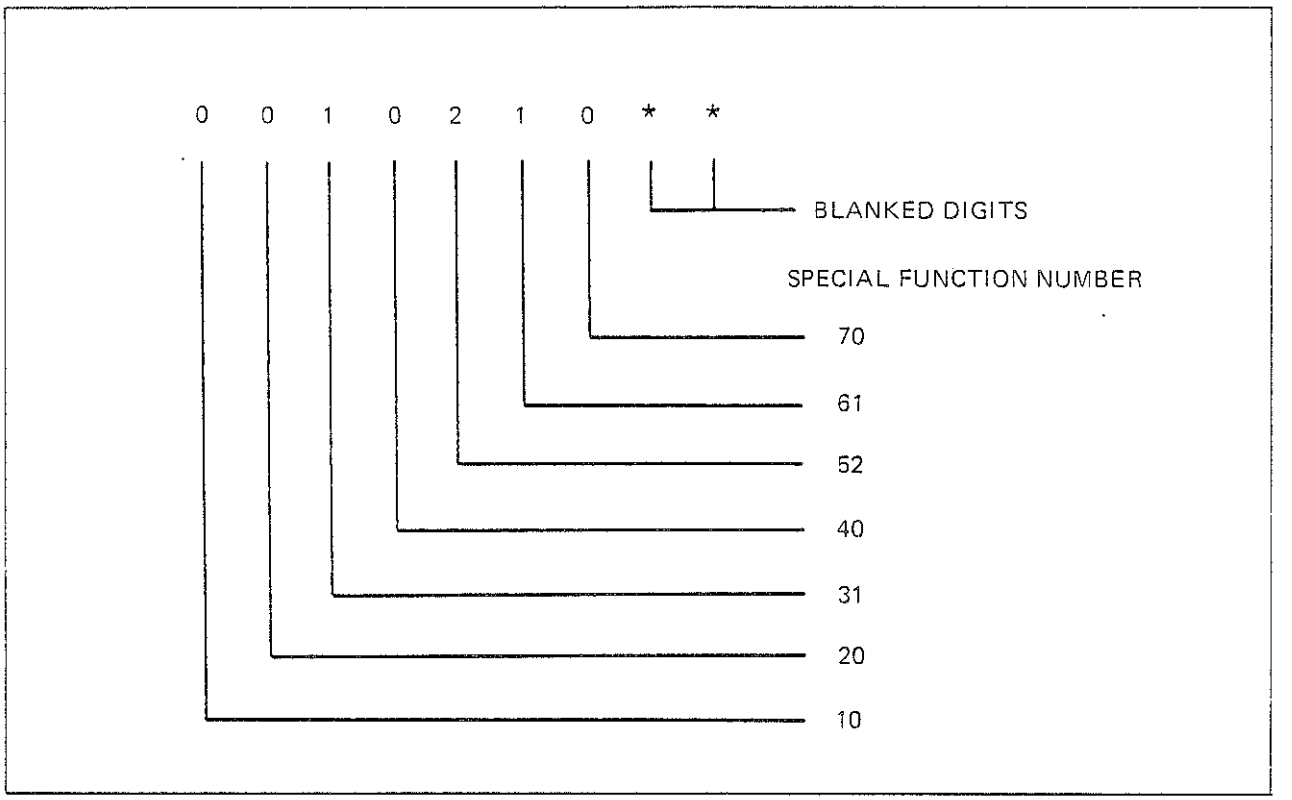


Figure 3.2 - Special Function Register Display

3.8.3 Setting the Special Function Register

3.8.3.1 Before a special function can be used, its unique number must first be entered into the special function register. Use key sequence:

[N] [N] [SHIFT] [STORE] [SF]

where NN is the special function number to be stored. The digits enter the display as the keys are pressed. The instrument returns to the measurement mode automatically once the special function number is stored.

3.8.3.2 When a special function number is stored, it overwrites the number stored in the same decade. To remove a number from the register, another special function number from the same decade must be stored.

3.8.3.3 The numbers stored in the register are retained while the instrument is in the standby mode.

3.8.4 Enabling and Disabling the Special Functions

3.8.4.1 The default state corresponds to the default state of the special function register, i.e., with Special Functions 10, 20, 30, 40, 50, 60, and 70 enabled. Special functions whose numbers are entered in the special function register are enabled and disabled using the following key sequence:

[SHIFT] [SF]

The SF LED lights when special functions is enabled.

NOTE:

A special function entered into its register while the special functions are enabled will be enabled immediately.

3.9 ERROR CODES

3.9.1 The instrument is able to detect a number of error states which are indicated on the display. Table 3.13 list the meanings of the various error codes.

Table 3.13 - Error Codes

Display	Error Description
Er 01	Phase measurement attempted on signals of different frequencies
Er 02	Measurement result too large for the display
Er 03	Overflow of internal counters
OP Er	Error in numerical entry
Er 50	Incorrect result obtained when in Check mode
Er 51	Relay or amplifier failure: Channel A: x10/x1
Er 52	Relay or amplifier failure: Channel A: 50Ω/1 MΩ
Er 53	Relay or amplifier failure: Channel A: DC/AC
Er 54	Relay or amplifier failure: Channel A: FILTER
Er 55	Relay or amplifier failure: COM A
Er 56	Relay or amplifier failure: Channel B: x10/x1
Er 57	Relay or amplifier failure: Channel B: 50Ω/1 MΩ
Er 58	Relay or amplifier failure: Channel B: DC/AC

NOTE:

Error codes Er 51 to Er 55 will only be generated with Special Function 77 active. Error codes Er 56 to Er 58 will only be generated with Special Function 78 active.

3.9.2 Clearing the Error Codes

3.9.2.1 Error code Er 01 is cleared by:

a. Making a phase measurement on signals of equal frequency

b. Selecting another measurement function

3.9.2.2 Error codes Er 02 and Er 03 are cleared by:

a. Obtaining a measurement result that is within range

b. Selecting another measurement function

3.9.2.3 OP Er is cleared by pressing [RESET]

3.10 MATH FUNCTION

3.10.1 General Information

3.10.1.1 The math function may be used with all measurement functions except Phase A rel B and CHECK. Its use permits the measured value to be offset and/or scaled before being displayed.

3.10.1.2 When the math function is active, the display indicates:

$$\frac{\text{Measurement Result} - X}{Z}$$

where X and Z are values entered by the operator into instrument stores. When the instrument is first powered on, X is set to 0 and Z to 1.

NOTE:

It is possible to set the constant Z to zero. However, any attempt to use the math function with this value set will cause an error code to be generated.

3.10.1.3 Table 3.14 shows how to set constants X and Z to obtain displays of ratio, offset (null), and percentage difference.

Table 3.14 - Uses of Math Function

Function Displayed	X	Z
Ratio: Measurement/N	0	N
Offset: Measurement - N	N	1
Percentage difference: 100 (Measurement-N)/N	N	N/100

3.10.2 Displaying the Math Constants

3.10.2.1 The values held in the X and Z stores can be displayed by pressing either

[SHIFT] [RECALL] [X] or

[SHIFT] [RECALL] [Z]

3.10.3 Changing the Math Constants

3.10.3.1 New values are entered into the math-constant stores using the numeric keypad. Employ either direct decimal or exponential format. For example, a value for X of 0.0231 may be entered using one of the following key sequences:

[.] [0] [2] [3] [1] [SHIFT] [STORE] [X]

or [2] [3] [1] [SHIFT] [EXP] [4] [SHIFT] [+/-] [SHIFT] [STORE] [X]

The instrument returns to the measurement mode automatically once the new math constant is stored.

3.10.3.2 The ranges of permissible values are as follows:

a. $1 \times 10^{-9} \leq Z < 1 \times 10^{10}$

b. 0

c. $-1 \times 10^{10} < Z \leq -1 \times 10^{-9}$

For negative numbers, the ninth digit is available, but not displayed.

3.10.4 Enabling and Disabling the Math Function

3.10.4.1 The math function is enabled and disabled by means of the key sequence

SHIFT (R-X)/Z

The (R-X)/Z LED lights when the function is enabled.

3.11 EXTERNAL ARMING

3.11.1 General Information

3.11.1.1 This features allows the start and/or stop point to be synchronized to a real-time event or complex signal. The arming signal is connected to the rear-panel input and the relevant special function selected (see Table 3.12). Measurement gate opening and closing are still determined by the input signal, but now can be conditioned (armed) by the external arming signal. Minimum start-to-stop external arming period is 50 μs (80 μs for RATIO A/B).

4.1 MATE/CIIL INTERFACE

4.1.1 Introduction

4.1.1.1 This subsection defines and describes the MATE/CIIL interface used on Racal-Dana Model 1992-02M.

4.1.2 CIIL Commands

4.1.2.1 Channel Assignments

4.1.2.1.1 Port numbers 0/00, 1/01, and 2/02 correspond to Channels A, B, and C, respectively, (i.e., Port = :CHn where n is the port number as just defined). Channels 0 and 1 are used for timing and frequency measurements up to 160 and 100 MHz, respectively. Channel 2 provides for high-frequency measurements up to 1.3 GHz. Arming is effected through a rear-panel channel (see Subsection 3.11).

4.1.2.2 Op Codes

4.1.2.2.1 Table 4.1 lists the op codes accepted and processed by the MATE interface. SET, SRX, and SRN op codes* may be used with any noun modifier shown in Table 4.6. The branched syntax diagrams (see Figures 4.1 - 4.7) show a choice of SET, SRX, and SRN op codes in typical setup. This does not impose or imply any constraint or ordering in the use of these three op codes. (The diagrams are programming examples only, not strict syntax.)

Table 4.1 - Applicable MATE/CIIL Op Codes

OP CODE	DESCRIPTION
FNC	Function
SET*	Set
SRX*	Set Maximum
SRN*	Set Minimum
CLS	Close
OPN	Open
INX	Initiate Measurement
STA	Status Request
FTH	Transmit Data
RST	Reset
IST	Execute Self Test
CNF	Execute Confidence Test

4.1.2.2.2 Each op code is interpreted and executed in accordance with definitions stated in MATE Specification 2806763 (Rev. B). Also, the following specific actions are initiated by the IST and CNF op codes:

a. **IST** - upon receipt of this op code, the counter initiates the following tests:

1. RAM, LOW address = µP RAM
   RAM, HIGH address = static RAM (IC28)

2. ROM - a 16-bit checksum is performed on the entire ROM

3. Functional - a check is made of the counter's ability to take a reading. The counter is placed into the 'Check' function, a reading is taken, and the result is then validated

After successful completion of these tests, the response to a STA (Status Request) command will be <space> <cr> <lf>. If any test fails, an error message will result from a STA command (see Subsection 4.1.5). To allow for IST execution time, wait approximately 1 second before requesting the status.

b. **CNF** - causes execution of the Functional Check described above in paragraph a.3

4.1.2.3 Nouns and Associated Measurements

4.1.2.3.1 Table 4.2 lists the nouns processed by the counter along with their allowed measurements and input ports.

Table 4.2 - Nouns and Associated Measurements/Port Numbers

NOUN	MEASUREMENT	PORT NUMBER
ACS	FREQ	00, 01, 02
	FRQR	00/01, 02/01
	PANG	00 rel 01
	PERI	00, 01
EVT	COUN	00
PDC	PANG	00 rel 01
	PERI	00, 01
	PRFR	00, 01
RPS, TRI, SQW	FREQ	00, 01
	FRQR	00, 01
	PANG	00 rel 01
	PERI	00, 01
DCS	ACCF	00, 01
TMI	TIME	00
PAC, PAT FMS, PMS, AMS	CFRQ	00, 01

4.1.2.4 Counter Setup Parameters

4.1.2.4.1 Noun modifiers either intrinsically specify the setup configuration of the counter (see Table 4.3) or, more commonly, a particular test-signal characteristic which then is used by the counter to determine its setup (see Table 4.4). Table 4.5 provides a compliance matrix for nouns and their measured characteristics. Also, Table 4.6 provides a compliance matrix for noun modifiers and their measured characteristics. Listings of measured characteristic and noun modifier ranges are contained in Table 4.7 and 4.8, respectively. Finally, use the glossary in Table 4.12 for definitions of noun modifiers and other important terms.

Table 4.3 - Noun Modifiers/Direct Counter Setup

NOUN MODIFIER	DESCRIPTION
ACPL/DCPL	Sets input coupling to AC/DC
BAND <value>	Sets the filter on if the <value> is ≤ 50 kHz; generates an error if the <value> is > 50 kHz. The default state is filter off
TIMP <value>	Sets input impedance to <value> ohms. The <value> is restricted to 50 or 1e6 for ports 00 and 01 and to 50 for port 02
RIMP <value>	When performing frequency ratio, phase, or event measurements, set the input impedance of the denominator or reference channel to <value> ohms. The <value> is restricted to 50 or 1e6 for ports 00 and 01. This noun modifier is an extension to MATE Specification 2806763 (Rev. B)
TRLV <value>	Sets trigger level to <value> volts. Trigger levels will be rounded up as follows: a. x1 attenuation - to next multiple of 20 mV b. x10 attenuation - to next multiple of 200 mV
TRSL POS/NEG	Sets trigger slope to positive or negative
NEGS/POSS	When used with an EVT noun, it has the same meaning as TRSL POS/NEG
GASC INT/ENT	Selects internal/external gate source
GAWD <value>	Sets internal gate to <value> seconds
GSTA POS/NEG	Used when in external gate. Sets gate to start on positive/negative slope of external gating signal. When used with COUN, sets the Channel B start slope
GSTO POS/NEG	Used when in external gate. Sets gate to stop on positive/negative slope of external gating signal. When used with COUN, sets the Channel B stop slope
MAXT <value>	Interpreted by the counter to be the maximum time expected for signal event to arrive at input ports after receipt of INX
SYNI	Used to indicate that an external synchronization signal will be used to start the measurement (always a TTL-crossing triggering, positive slope)

Table 4.4 - Noun Modifiers/Indirect Counter Setup

NOUN MODIFIER	DESCRIPTION
<meas chr> <value>	When the measurement characteristic of the current setup is received, the information is compared against the capabilities of the counter to determine validity of the setup. In addition, when applicable, the value is used in the calculation of the timeout number sent to the computer in response to an INX op code (see MATE Specification 2806763 (Rev. B, Section 5.3.2.1.1)
VLPP <value>	Voltage peak-to-peak of the input signal. Used to determine attenuation range of input channels when auto-trigger is not active. To accommodate the "loose" usage of this parameter in ATLAS, VLPP means VLPK for PDC, PDT, and STS
VLPK <value>	Voltage peak of the input signal. Used to determine attenuation range of input channels when auto-trigger is not active
DCOF <value>	DC offset of the input signal. Used to determine attenuation range of input channels when auto-trigger is not active
VOLT <value>	RMS value of AC input signal. Used to determine attenuation range of input channels when auto-trigger is not active. To accommodate the "loose" usage of this parameter in ATLAS, "VOLT" means VLPK for all signals except ACS, TRI, and SQW
REFV <value>	When making frequency ratio, phase, or event measurements, this parameter is used to determine input voltage range of the denominator or reference channel. This noun modifier is an extension to MATE Specification 2806763 (Rev. B)

Table 4.5 - Noun/Measured Characteristic Compliance Matrix

MEASURED CHARACTERISTIC	NOUN														
	ACS	AMS	DCS	EVT	FMS	PAC	PAT	PDC	PDT	PMS	RPS	SQW	STS	TMI	TRI
ACCF	N	N	Y	N	N	N	N	N	N	N	N	N	N	N	N
CFRQ	N	Y	N	N	Y	Y	Y	N	N	Y	N	N	N	N	N
COUN	N	N	N	Y	N	N	N	N	N	N	N	N	N	N	N
FREQ	Y	N	N	N	N	N	N	N	N	N	Y	Y	N	N	Y
FRQR	Y	N	N	N	N	N	N	N	N	N	Y	Y	N	N	Y
PANG	Y	N	N	N	N	N	N	Y	N	N	Y	Y	N	N	Y
PERI	Y	N	N	N	N	N	N	Y	N	N	Y	Y	N	N	Y
PRFR	N	N	N	N	N	N	N	Y	N	N	N	N	N	N	N
TIME	N	N	N	N	N	N	N	N	N	N	N	N	N	Y	N
VLPK (TMI)	Y	N	N	N	N	N	N	Y	Y	N	Y	Y	Y	N	Y
VLPP (TMI)	Y	N	N	N	N	N	N	Y	Y	N	Y	Y	Y	N	Y
VOLT (TMI)	Y	N	N	N	N	N	N	Y	Y	N	Y	Y	Y	N	Y

KEY:
Y = Valid Noun/Measured Characteristic Combination
N = Invalid Noun/Measured Characteristic Combination

Table 4.6 - Noun Modifier/Measured Characteristic Compliance Matrix

NOUN MODIFIER	MEASURED CHARACTERISTIC											
	ACCF	CFRQ	COUN	FREQ	FRQR	PANG	PERI	PRFR	TIME	VLPK(TMI)	VLPP(TMI)	VOLT(TMI)
ACPL	A	A	A	A	A	A	A	A	I	A	A	A
BAND	A	A	A	A	A	A	A	A	A	A	A	A
CLKO	I	I	I	I	I	I	I	I	I	I	I	I
DCOF	A	A	A	A	A	A	A	A	I	A	A	A
DCPL	A	A	A	A	A	A	A	A	I	A	A	A
GASC EXT	A	A	A	A	A	I	A	A	I	I	I	I
GASC INT	A	A	I	A	A	I	A	A	I	I	I	I
GAWD	A	A	I	A	A	I	A	A	I	I	I	I
GSTA NEG	A	A	A	A	A	I	A	A	I	I	I	I
GSTA POS	A	A	A	A	A	I	A	A	I	I	I	I
GSTO NEG	A	A	A	A	A	I	A	A	I	I	I	I
GSTO POS	A	A	A	A	A	I	A	A	I	I	I	I
MAXT	A	A	A	A	A	A	A	A	A	A	A	A
NEGS	D	D	A	D	D	D	D	D	D	D	D	D
POSS	D	D	A	D	D	D	D	D	D	D	D	D
REFV	D	D	A	D	A	A	D	D	D	D	D	D
RIMP	D	D	A	D	A	A	D	D	D	D	D	D
SAMA	D	D	D	D	D	D	D	D	D	D	D	D
SYNI	A	A	A	A	A	I	A	A	A	A	A	A
TIME	D	D	D	D	D	D	D	D	D	D	D	D
TIMP	A	A	A	A	A	A	A	A	I	A	A	A
TRSC EXT	D	D	D	D	D	D	D	D	D	D	D	D
TRSC INT	I	I	I	I	I	I	I	I	I	I	I	I
TRLV	A	A	A	A	A	A	A	A	I	R	R	R
TRSL	A	A	A	A	A	A	A	A	I	A	A	A
VLPK	A	A	A	A	A	A	A	A	I	A	A	A
VLPP	A	A	A	A	A	A	A	A	I	A	A	A
VOLT	A	A	A	A	A	A	A	A	I	A	A	A

NOTE:

Each element of the matrix may contain one of the following:

D = Noun Modifier and Measured Characteristic Combination is Disallowed
A = Noun Modifier and Measured Characteristic Combination is Allowed
I = No Action Required
R = Noun Modifier Must Be Present in Setup String

Table 4.7 - Noun Modifier Ranges/Measured Characteristic

MEASURED CHARACTERISTIC	CHANNELS 00, 01		CHANNEL 02	
	MIN (for 01)	MAX (for 01)	MIN	MAX
ACCF	1e-3 *1	1.6e8 (1e8)	4e7	1.3e9
CFRQ	1e-3 *1	1.6e8 (1e8)	4e7	1.3e9
COUN	0	1e18-1	—	—
FREQ	1e-3 *1	1.6e8 (1e8)	4e7	1.3e9
FRQR	1e-11 *2	1.6e11	4e-1	1.3e12
PANG	0	3.599e2	—	—
PERI	6.25e-9 (1e-8)	1e3 *2	—	—
PRFR	1e-3 *1	1.6e8 (1e8)	4e7	1.3e9
TIME	0	1e3	—	—
For SQW Signal:				
VLPP (TMI)	1.0e-1	1.02e2 *4	—	—
|VLPK| (TMI)	5.0e-2	1.02e2 *4	—	—
VOLT (TMI)	2.5e-2	5.1e1 *4	—	—
For TRI Signal:				
VLPP (TMI)	8.6e-2	1.76e2 *4	—	—
|VLPK| (TMI)	4.3e-2	8.8e1 *4	—	—
VOLT (TMI)	2.5e-2	5.1e1 *4	—	—
For ACS & All Other Signals				
VLPP (TMI)	7.2e-2	1.48e2 *4	—	—
|VLPK| (TMI)	3.6e-2	7.2e1 *4	—	—
VOLT (TMI)	2.5e-2	5.1e1 *4	—	—

See NOTES 1 and 2 after Table 4.8

Table 4.8 - Noun Modifier Ranges

NOUN MODIFIERS	CHANNELS 00, 01		CHANNEL 02	
	MIN	MAX	MIN	MAX
BAND	0	50e3	—	—
DCOF	-5.1e1	5.1e1 *4	—	—
GAWD	1e-3	1e1	1e-3	1e1
MAXT	1e-2	9.999e3	1e-2	9.999e3
RIMP	5e1	1e6	—	—
TIMP	5e1	1e6	5e1	5e1
TRLV	-5e1	5e1	0	0
For SQW Signal:				
VLPP (or REFV)	1.0e-1	1.02e2 *4	—	—
|VLPK| (or REFV)	5.0e-2	1.02e2 *4	—	—
VOLT (or REFV)	2.5e-2	5.1e1 *4	—	—
For TRI Signal:				
VLPP (or REFV)	8.6e-2	1.76e2 *4	—	—
|VLPK| (or REFV)	4.3e-2	8.8e1 *4	—	—
VOLT (or REFV)	2.5e-2	5.1e1 *4	—	—
For ACS & All Other Signals:				
VLPP (or REFV)	7.2e-2	1.48e2 *4	2.8e-2	1.98e1 *3
|VLPK| (or REFV)	3.6e-2	7.2e1 *4	1.4e-2	9.9e0 *3
VOLT (or REFV)	2.5e-2	5.1e1 *4	1e-2	7e0 *3

NOTE 1:

The maximum combination values for Voltage and DC offset with a TIMP value of 1e6 ohms and DC coupling are as follows:

For SQW Signal:

$$\frac{(VLPK)^2}{4} + (DCOF)^2 \leq (51)^2$$

For TRI Signal:

$$\frac{(VLPK)^2}{3} + (DCOF)^2 \leq (51)^2$$

For ACS & All Other Signals:

$$\frac{(VLPK)^2}{2} + (DCOF)^2 \leq (51)^2$$

NOTE 2:

The maximum combination values for Voltage and DC offset with a TIMP value of 50 ohms and DC coupling are as follows:

For SQW Signal:

$$\frac{(VLPK)^2}{4} + (DCOF)^2 \leq (5)^2$$

For TRI Signal:

$$\frac{(VLPK)^2}{3} + (DCOF)^2 \leq (5)^2$$

For ACS & All Other Signals:

$$\frac{(VLPK)^2}{2} + (DCOF)^2 \leq (5)^2$$

*1 MIN of 50 applies if trigger level is not specified
*2 MIN value for frequencies of signals is the same as FREQ
*3 AC sinewave input
*4 For TIMP value of 1e6 ohms. For a TIMP value of 50 ohms, the following maximum values apply:

Noun Modifier	Maximum
DCOF	5e0
VLPK SQW Signal	1.0e1
VLPK TRI Signal	8.6e0
VLPK Other Signals	7e0

4.1.3 Programming Constructs

4.1.3.1 The general construct for counter setup starts with a string containing an FNC op code, followed by a sequence of SET, SRX, or SRN op codes. This single string is terminated by an ASCII carriage return (cr) and line feed (lf).

4.1.3.2 For TMI measurements, the FNC setup string is followed by two more FNC strings; the first for the start channel, the second for the stop channel. Setup execution, measurement retrieval, and instrument reset are all programmed in accordance with MATE Specification 2806763 (Rev. B), Section 5.3.3.1.1.

4.1.3.3 Tables 4.9 and 4.10 show valid constructs, while Figures 4.1 - 4.7 provide branched syntax charts for all measurements.

Table 4.9 - Single FNC Setup

```
FNC <noun><measurement characteristic><port>
SRX <measurement characteristic><value>
SRN <measurement characteristic><value>
SET <noun modifier>[<value>]
•
•
SET <noun modifier>[<value>]
cr lf

INX <measurement characteristic>
cr lf

FTH <measurement characteristic>
cr lf

RST <noun><measurement characteristic><port>
cr lf
```

Table 4.10 - Time Interval FNC Setup

```
FNC TMI <measurement characteristic>:CH0
SRX <measurement characteristic><value>
SRN <measurement characteristic><value>
SET <noun modifier>[<value>]
•
•
SET <noun modifier>[<value>]
cr lf

FNC<noun><voltage measurement characteristic><port>
SRX<measurement characteristic><value>
SRN<measurement characteristic><value>
SET<modifier>[<value>]
•
•
SET <noun modifier>[<value>]
cr lf
```

le 4.10 - Time Interval FNC Setup (Cont'd)

```
FNC <noun><voltage measurement characteristic><port>
SRX <measurement characteristic> <value>
SRN <measurement characteristic> <value>
SET <noun modifier>[<value>]
•
•
SET <noun modifier>[<value>]
cr lf

INX <measurement characteristic>
cr lf

FTH <measurement characteristic>
cr lf

RST <noun><measurement characteristic><port>
cr lf
```

4.1.4 Normal Response Output Format

4.1.4.1 Normal Output - Response to FTH

4.1.4.1.1 The following is a description of a normal ASCII output string for measurement data:

Byte Number	Description
1	space
2	sign (+ or -)
3	digit (0-9)
4-14	10 digits with decimal point (0-9)
15	letter E
16	sign (+ or -)
17	digit (0-9) } exponent will always be
18	digit (0-9) } a multiple of three
19	CR
20	LF

4.1.4.2 Normal Output - Timeout Response to INX

Byte Number	Description
1	space
2-5	digit (0-9)
6	CR
7	LF

4.1.4.3 Normal Output - Status Response to STA

Byte Number	Description
1	space
2	CR
3	LF

4.1.5 Abnormal Response Output Format

4.1.5.1 The format for all abnormal responses is as follows:

F ⟨digit⟩ ⟨digit⟩ FTM00 ⟨space⟩ (⟨origin⟩) ⟨message⟩⟨CR⟩⟨LF⟩

a. FTM = Module Name

b. ⟨digit⟩ ⟨digit⟩ are defined as follows:
05 = Measurement Timeout
06 = Trigger/Gate/External Reference not received
07 = Syntax, IST/CNF, noncatastrophic failure

c. ⟨origin⟩ is defined as:
MOD = Error detected in counter's control section
DEV = Error detected in counter's measurement section

4.1.5.2 The following string may be transmitted as a result of an error having occurred:

F07FTM00: ERROR NUMBER # #

4.1.5.3 A list of the error numbers that may be transmitted is provided in Table 4.11.

Table 4.11 - MATE Syntax Error Numbers

NUMBER	ERROR
1	Phase measurement attempted on waveforms of differing frequency
2	Result out-of-range of the display
3	Overflow of internal counters
4	Error in numerical entry
5	Syntax error in command
6	Low address RAM (inside µP) failed
7	High address RAM (IC28) failed
8	ROM checksum failed
9	CNF failed
11	The op code is not recognized
12	A Line Feed was not found as expected in the CIIL input string
13	The noun is not recognized
14	The measurement characteristic is not recognized

Table 4.11 - MATE Syntax Error Numbers (Cont'd)

NUMBER	ERROR
15	The channel number expression contains a syntax error
16	The channel number is out-of-range
17	The noun/measurement characteristic combination is invalid
18	The modifier/measurement characteristic combination is invalid
19	Neither POS nor NEG was found when expected
21	Slope must be set to POS for Channel C
22	Measurement characteristic of TMI start and stop channels are not the same
23	TMI start channel is not channel 00 (A)
24	INX or FTH found while parsing a FNC statement
25	STA, CNF, or IST found while parsing a FNC statement
26	RST found while parsing a FNC statement
27	OPN or CLS found while parsing FNC statement
28	Measurement characteristic must be VLPP, VLPK, or VOLT for start/stop TMI channel
29	Gate source (Channel B) must be EXT for event measurement
30	Neither EXT nor INT found when expected
31	Only DC-coupling allowed with Channel C measurement
33	Gate start and stop slopes must be opposite for COUN
34	Number is out-of-range (larger than 9.9e17)
35	Syntax in numeric expression
36	Channel C impedance must be 50 ohms
37	Neither 50 ohms nor 1e6 ohms found for impedance
38	Maximum number of characters (15) exceeded on input word
39	Channel C trigger level must be zero
40	Trigger level is out-of-range (-51 to +51 is valid)
41	DC offset value is out-of-range (-51 to +51 is valid)
42	VLPK (or VOLT, or VLPP) is out-of-range
43	VLPP must be a positive number
44	Voltage too large with impedance of 50
45	DCOF value too large with impedance of 50
46	Ch 0 DCOF and voltage combined too large for impedance
47	Ch 1 DCOF and voltage combined too large for impedance
48	Ch 0 TRLV out-of-range for DCOF and voltage
49	Ch 1 TRLV out-of-range for DCOF and voltage
50	SRN/SRX value is too small for COUN measurement characteristic
51	SRN/SRX value is too small for measurement characteristic
52	SRN/SRX value is too large for measurement characteristic
53	MAXT value is too large
54	MAXT value is too small
55	GAWD value is too small
56	GAWD value is too large
57	BAND value is too large
58	BAND value is too small

Table 4.11 - MATE Syntax Error Numbers (Cont'd)

NUMBER	ERROR
59	TRSC must be INTernal and not EXTernal
60	FTH op code found before INX was received
61	Neither SRX nor SRN op code found
63	Neither SRX nor SRN found for TMI start and/or stop channel
64	SET TRLV not found for TMI start and/or stop channel
65	SET VOLT, VLPP nor VLPK found for measurement characteristic
66	Reading timed out - signal not found or measurement not in specified time
67	SET TIME noun modifier not allowed

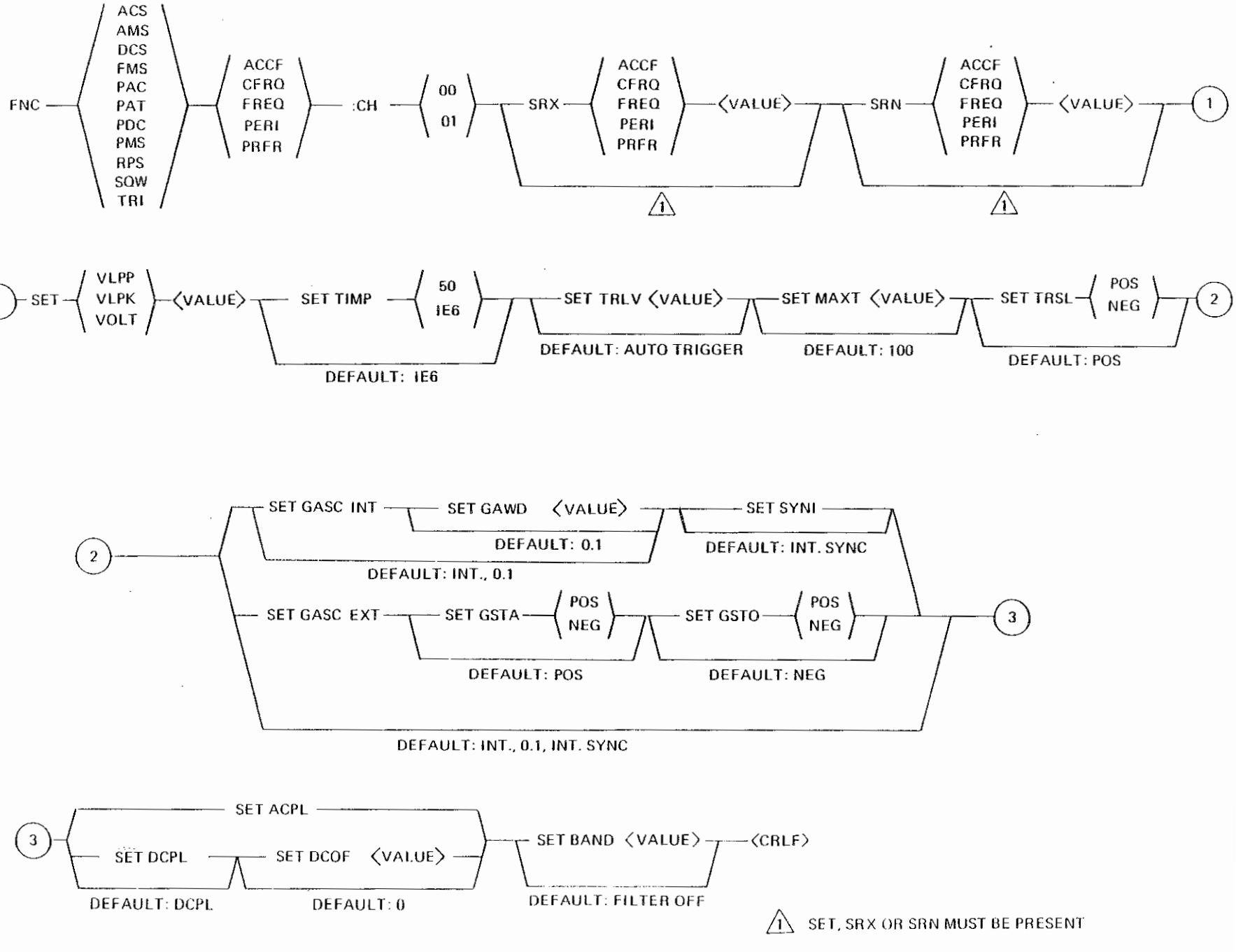


Figure 4.1 – Frequency, Period, and Pulse Rep. Rate (Ports 00, 01)

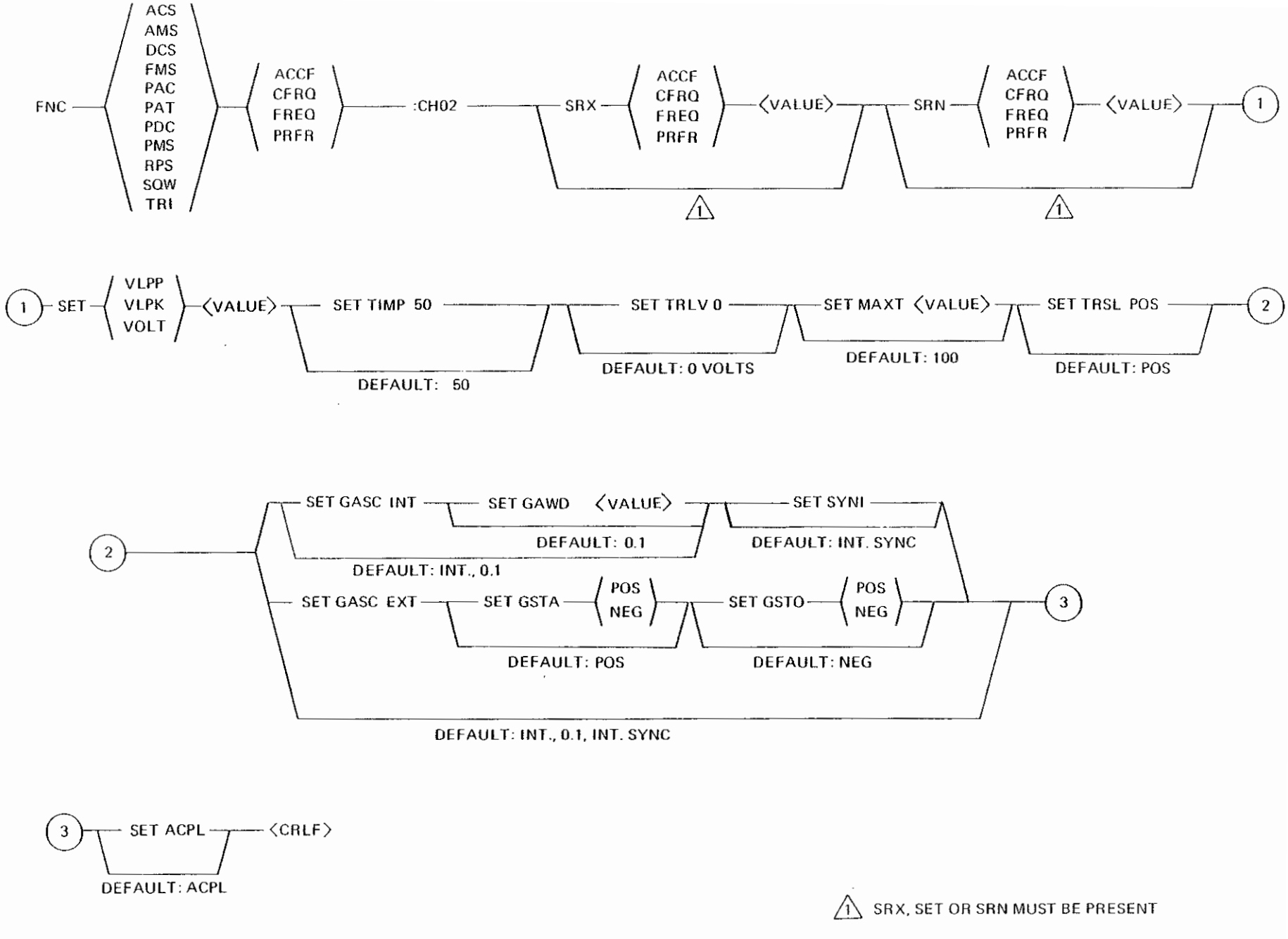


Figure 4.2 – Frequency and Pulse Rep. Rate (Port 02)

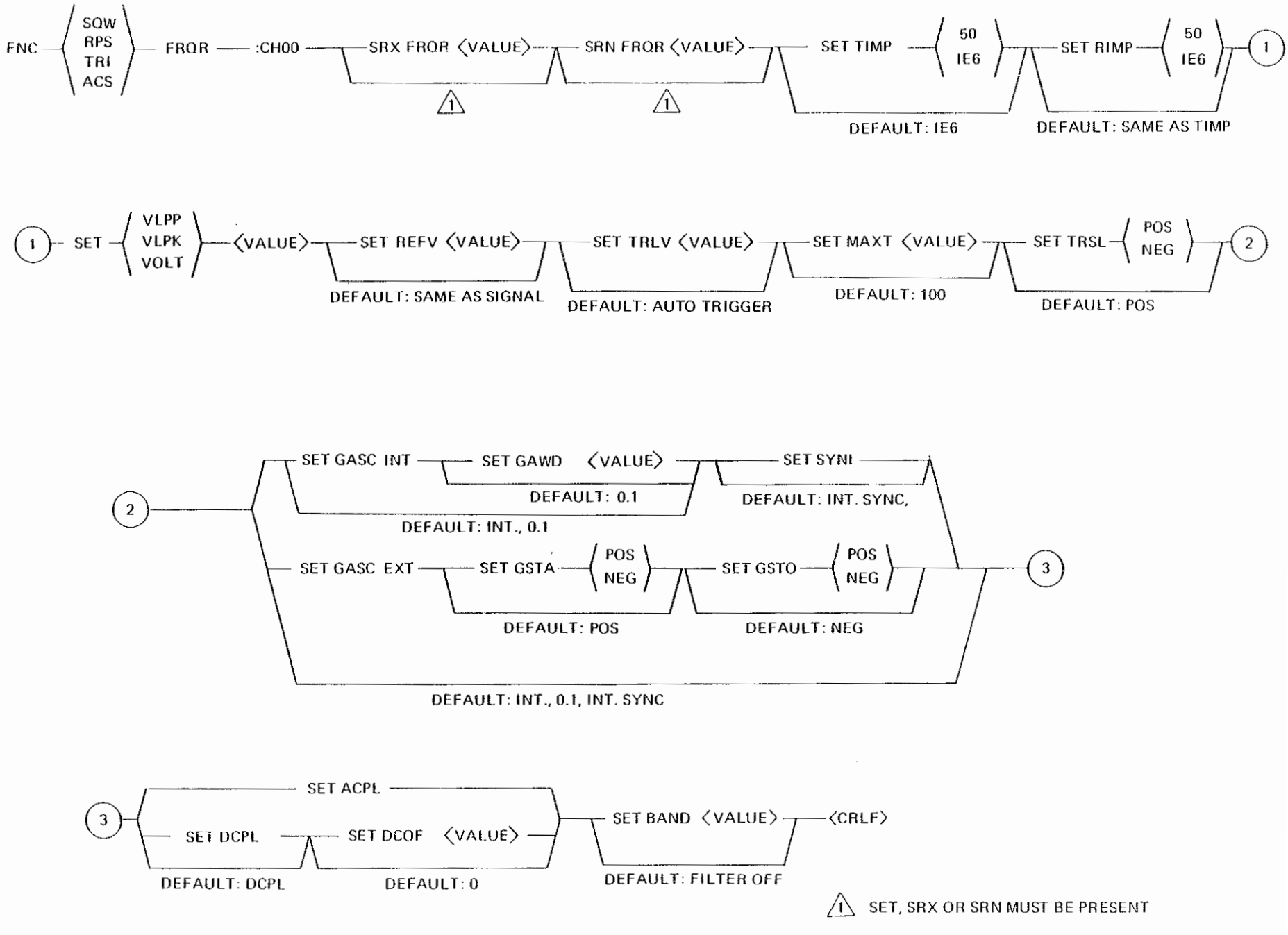


Figure 4.3 – Frequency Ratio (Port 00)

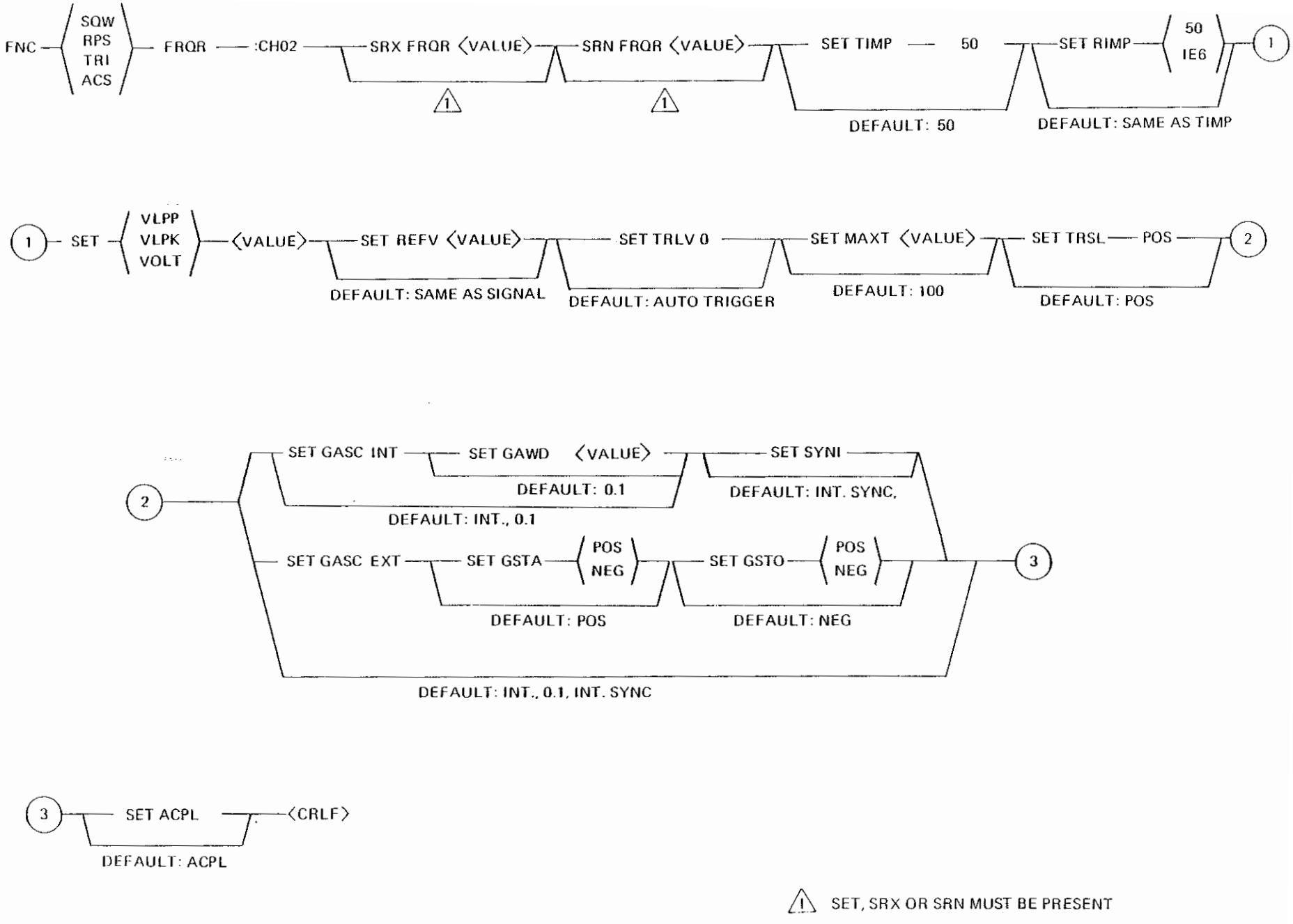


Figure 4.4 – Frequency Ratio (Port 02)

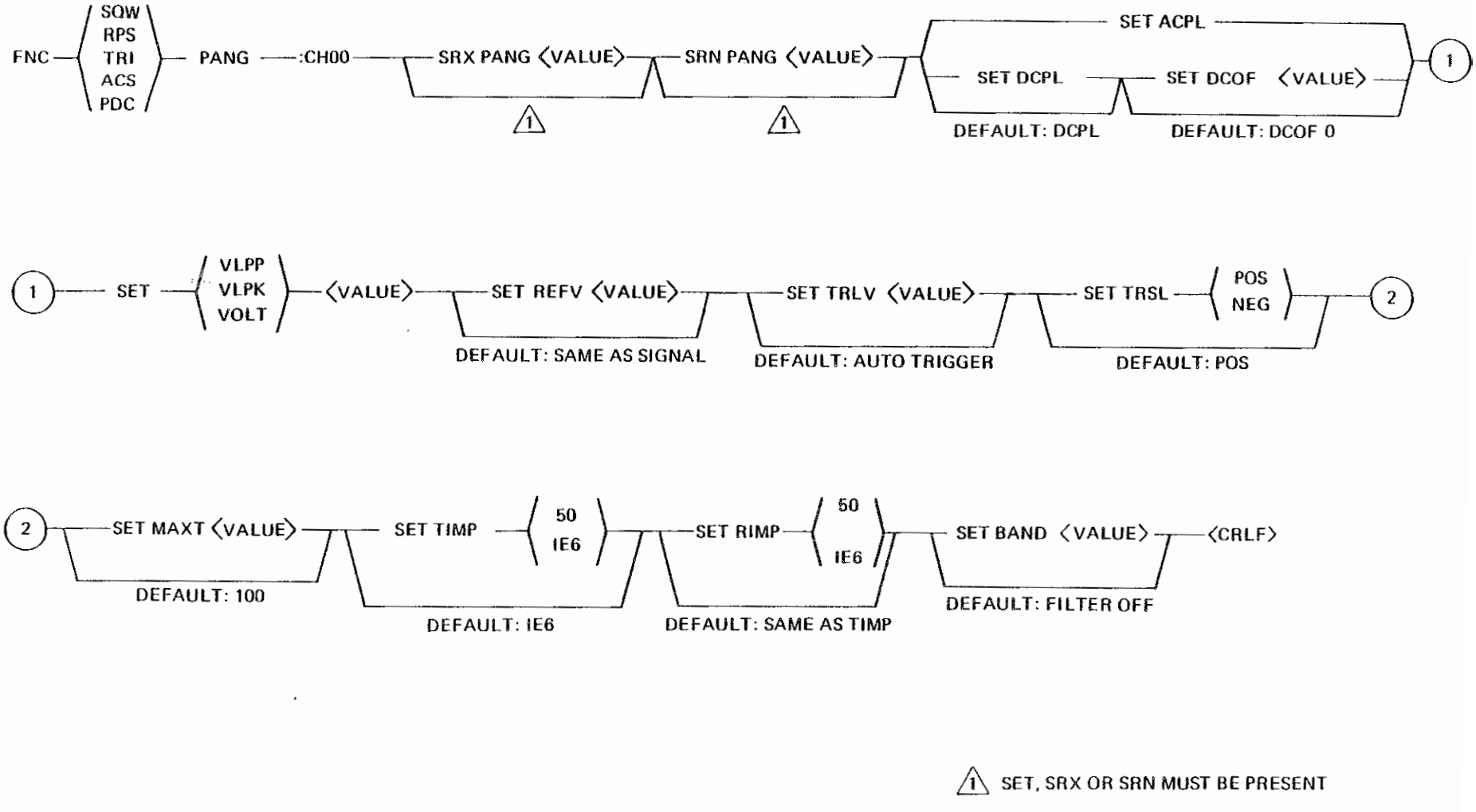


Figure 4.5 – Phase Measurement

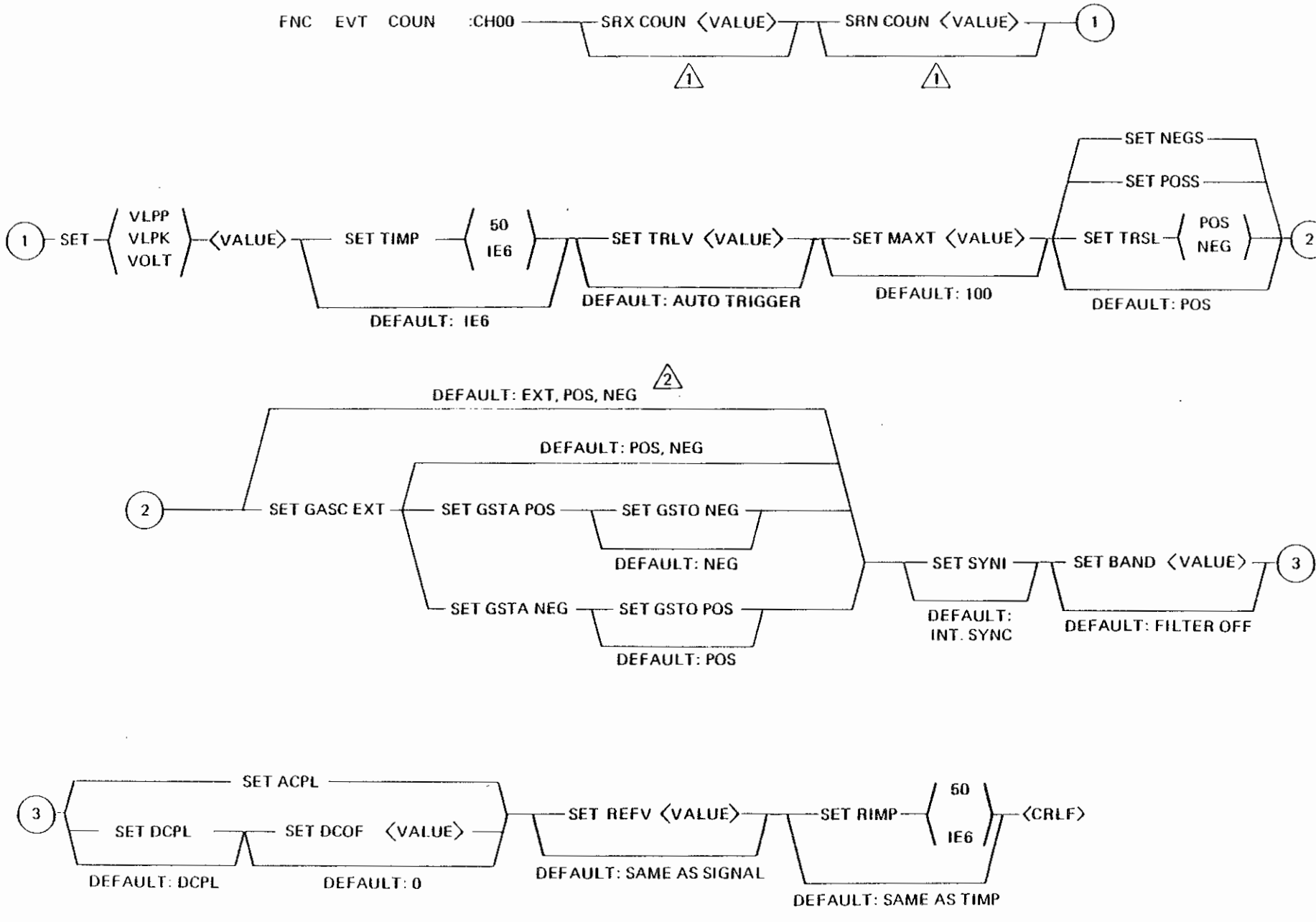


Figure 4.6 – Event Measurement

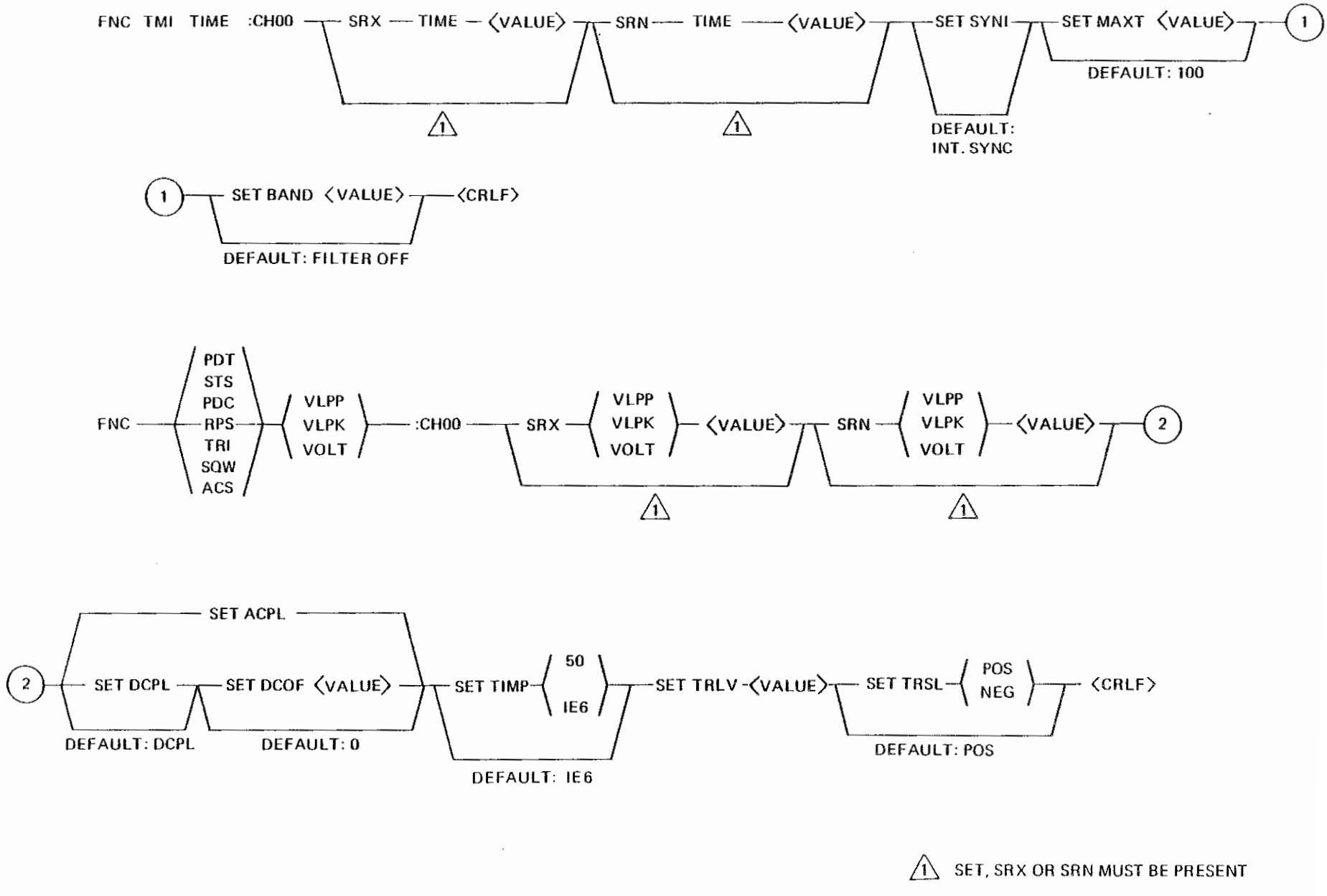
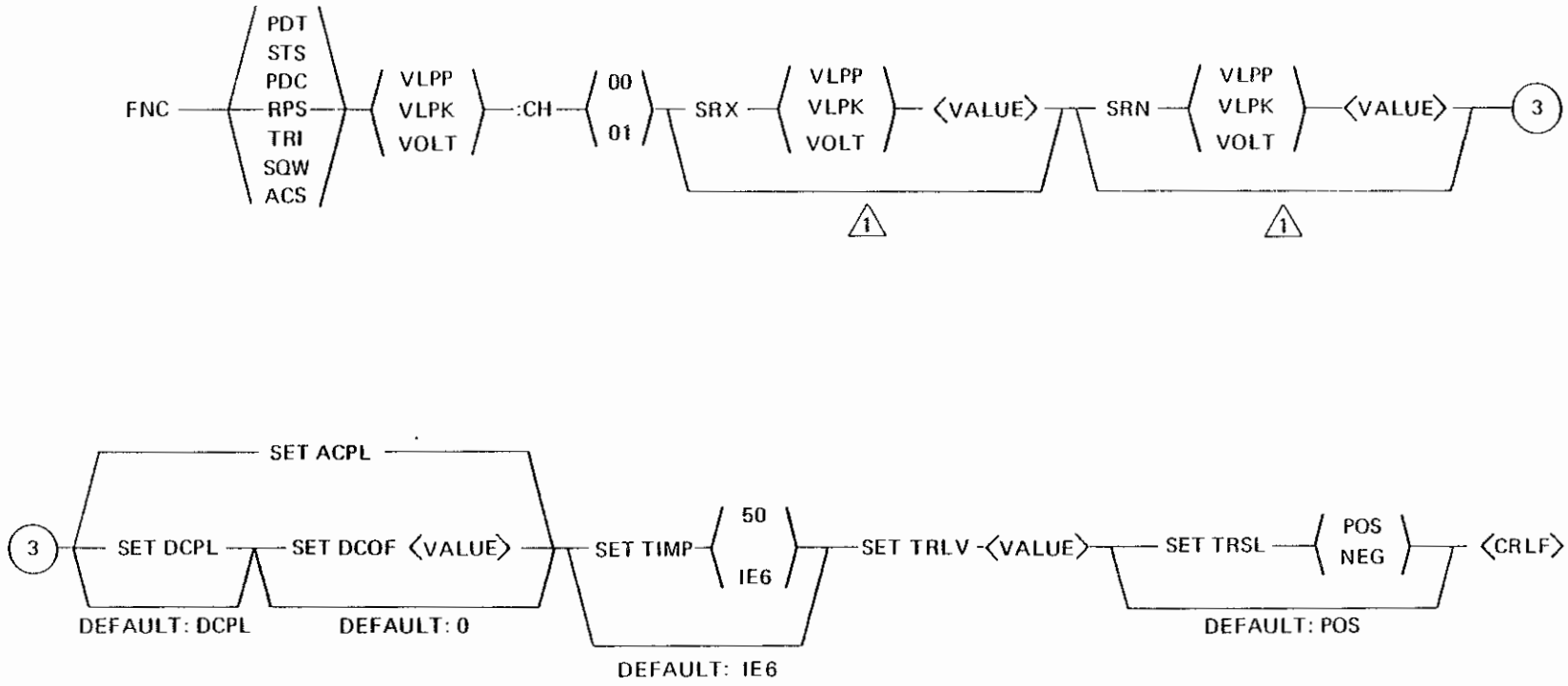


Figure 4.7 - Time Interval



1 SET, SRX OR SRN MUST BE PRESENT

Figure 4.7 – Time Interval (Cont'd)

4.1.6 Timeout Values

4.1.6.1 Timeout values are calculated when an INX instruction is received and transmitted when the counter is made into a talker. The value depends on the function:

4.1.6.2 For phase angle, frequency ratio, and event counts (COUN, FRQR, PANG) use:

Timeout = MAXT <value> + 204 seconds

4.1.6.3 For frequency-related functions (ACCF, CFRQ, FREQ, PRFR) use:

Timeout = MAXT <value> + GAWD <value> + max $[2 \cdot (1/\text{freq}) + 4, 24]$
OR if externally gated:
Timeout = MAXT <value> + 100 seconds + max $[2 \cdot \text{peri} + 4, 24]$
where freq = the minimum value specified for SRX/SRN range

4.1.6.4 For period (PERI) use:

Timeout = MAXT <value> + GAWD <value> + max $[2 \cdot \text{peri} + 4, 24]$
OR if externally gated:
Timeout = MAXT <value> + 100 seconds + max $[2 \cdot (1/\text{freq}) + 4, 24]$
where peri = the maximum value specified for SRX/SRN range

4.1.6.5 For time (TIME) use:

Timeout = MAXT <value> + max $[2 \cdot \text{time} + 4, 24]$
where time = the maximum value specified for SRX/SRN range

Table 4.12 - Glossary of Terms

Nouns

ACS	(AC SIGNAL): A sinusoidal time-varying electrical potential
AMS	(AM SIGNAL): An amplitude modulated sinewave generated when the amplitude of one wave is varied in accordance with the amplitude of another wave.
DCS	(DC SIGNAL): An unvarying electrical potential.
EVT	(EVENTS): The occurrence of an electrical signal to be counted.
FMS	(FM SIGNAL): A frequency-modulated sinewave generated when the frequency of one wave is varied in accordance with the amplitude of another wave.
PAC	(PULSED AC): Pulsed alternating current signal. An EMF characterized by short duration periods of AC (sinusoidal) electrical potential.
PAT	(PULSED AC TRAIN): An EMF characterized by a train of different short duration periods of AC sinusoidal electrical potential.
PDC	(PULSED DC): Pulsed direct current signal. An EMF characterized by short duration periods of positive or negative electrical potential occurring either periodically or nonperiodically in time.
PDT	(PULSED DC TRAIN): An EMF characterized by a train of different single pulses with a defined time correlation between the single elements.
PMS	(PM SIGNAL phase-modulated signal): A phase-modulated signal is generated when the phase of one wave is varied in accordance with the amplitude of another wave.

Table 4.12 - Glossary of Terms (Cont'd)

Nouns

RPS	(RAMP SIGNAL): A varying EMF whose wave shape is characterized by a periodic series of alternately positive and negative linear amplitude slopes wherein the ratio of positive to negative slope does not equal one.
SQW	(SQUARE WAVE): A varying electrical potential whose waveshape is characterized by a periodic series of rectangles indicating alternately positive and negative potential.
STS	(STEP SIGNAL): A change of DC electrical potential from one level to another either positive or negative.
TMI	(TIME INTERVAL): The time between two events.
TRI	(TRIANGULAR WAVE SIGNAL): A varying electrical potential whose waveshape is characterized by a periodic series of alternately positive and negative linear slopes, wherein the ratio of positive to negative slope is equal to one.

Noun Modifiers

ACCF	(AC-COMP-FREQ): The frequency of an AC component voltage or current signal.
ACPL	(AC-COUPLE): Only the AC portion of the signal is to be analyzed. The DC portion is to be eliminated.
BAND	(BANDWIDTH): The difference between the upper and lower frequencies of a frequency selective circuit where 3 dB attenuation occurs.
CFRQ	(CAR-FREQ): The time-average frequency of the carrier wave signal in the absence of modulation.
COUN	(COUNT): Number of events or items.
DCOF	(DC-OFFSET): The DC voltage or current level of a defined reference base line. DCOF voltage or current is measured from zero volts to reference base line.

Table 4.12 - Glossary of Terms (Cont'd)

Noun Modifiers (Cont'd)

DCPL	(DC-COUPLE): Both the AC and DC portions of signal are to be analyzed.
FREQ	(FREQ): The rate at which a periodic electrical function is repeated, expressed in the unit Hertz.
FRQR	(FREQ-RATIO): The ratio of the frequencies of two signals.
GATO	(GATE-OUT): Defines a situation where an internally generated gating signal is to be output to the pin specified by the gate-out pin descriptor.
GASC	(GATE-SOURCE): Defines a gating pulse to be an internal or external signal. This modifier takes the values INT or EXT. In those cases when a gate-source is not specified the gate signal is assumed to be internal.
GAWD	(GATE-WIDTH): Defines the length of time for a gating signal. The time for which an instrument 'looks' at a signal in deriving a measurement.
GSTA	(GATE-START-SLOPE): Defines a start condition for a gating signal. This modifier takes the values POS or NEG.
GSTO	(GATE-STOP-SLOPE): Defines a stop condition for a gating signal. This modifier takes the values POS or NEG.
MAXT	(MAX-TIME): This modifier specifies an escape or override time delay that forces continuation of the test sequence in the event an expected UUT response does not occur.
NEGS	(NEG-SLOPE): The portion of a waveform having a negative derivative.
PANG	(PHASE-ANGLE): The angular difference expressed in degrees between the signal described by the noun and the signal referenced by the REF HI and REF LO pins.

able 4.12 - Glossary of Terms (Cont'd)

Noun Modifiers (Cont'd)

PERI	(PERIOD): The period (i.e., 1/frequency) of a waveform, pulse, or pulse train. Used as a statement characteristic or measured characteristic.
POSS	(POS-SLOPE): The portion of a waveform having a positive derivative.
PRFR	(PRF): The time rate at which pulses occur.
REFV	(REF-VOLTAGE): The input voltage of a reference signal when making a dual signal measurement (phase, frequency ratio).
RIMP	(REF-IMPEDANCE): The input impedance of a reference channel when making a dual signal measurement (phase, frequency ratio).
SYNI	(SYNC-IN): Noun modifier used to indicate external arming.
TIME	(TIME): The measurement of time using a standard time measurement function as a reference or the interval over which EVENTS are counted.
TIMP	(TEST-EQUIP-IMP): Internal impedance of the test equipment (i.e., the test output impedance for a SOURCE function; the test equipment input impedance for a SENSOR function).
TRSC	(TRIGGER SOURCE): Noun modifier used to indicate INT or EXT triggering.
TRLV	(TRIG-LEVEL): Defines the voltage level of the trigger signal.
TRSL	(TRIG-SLOPE): Defines whether the triggering level applies to the up or down slope of a signal. This modifier takes the values POS or NEG.
VLPK	(VOLTAGE-P):
VLPP	(VOLTAGE-PP):
VOLT	(VOLTAGE): An electrical potential. In the case of DC signals the potential is unvarying. In the case of AC signals it is the generally used parameter which assumes a distortionless sinusoidal signal for a valid rms value.

SECTION 5 GENERAL THEORY OF OPERATION

5.1 INTRODUCTION

5.1.1 This section describes the general theory of operation for the 1992-02M.

5.1.2 The theory of operation provided is based on the simplified overall block diagram shown in Figure 5.1. Key circuit blocks of the 1992-02M are described and supported in this section using simplified block and schematic diagrams. These diagrams supplement the complete schematics found in Section 7 of this manual. As much as possible, the simplified schematic and block diagrams provided here are annotated with the same reference designators found in the complete schematics. This should facilitate cross-referencing between this section of the manual and the schematics.

5.1.3 Integrated circuits (ICs) in the following circuit descriptions are designated by circuit references provided on the supporting simplified block and schematic diagrams. The IC designations employed in the following key circuit descriptions follow those found in supplied schematics.

When an IC package contains more than one circuit, suffix letters are used to distinguish them (e.g., IC1a). Finally, when it is necessary to identify a specific pin in an IC, the reference designator, with a suffix letter if necessary, is followed by a hyphen and then the required pin number (e.g., IC1a-1).

5.2 FUNCTIONAL BLOCKS

5.2.1 The 1992-02M contains the following ten main functional blocks:

a. Channel A/B block (see Subsection 5.3.1)

b. Channel C block (see Subsection 5.3.2)

c. Measurement block (see Subsection 5.3.3)

d. Display block (see Subsection 5.3.4)

e. Keyboard block (see Subsection 5.3.5)

f. Microprocessor block (see Subsection 5.3.6)

g. Standby and IRQ block (see Subsection 5.3.7)

h. Power Supply block (see Subsection 5.3.8)

i. Internal Frequency Standard block (see Subsection 5.3.9)

j. GPIB Interface (see Subsection 5.3.10)

5.2.2 The functional relationship between the blocks of the 1992-02M is illustrated in Figure 5.1. The measurement block is internally configured by the microprocessor according to the instructions entered via the keyboard or over the GPIB. The signal to be measured and the signal from the frequency standard are fed to the measurement block. The measured result is passed to the microprocessor. If mathematical manipulation of the result is required, this is performed by the microprocessor before the final output is passed to the display or system.

5.2.3 The standby and IRQ block handles instructions to switch to standby. These instructions are received from the keyboard block and interrupt requests made by other systems.

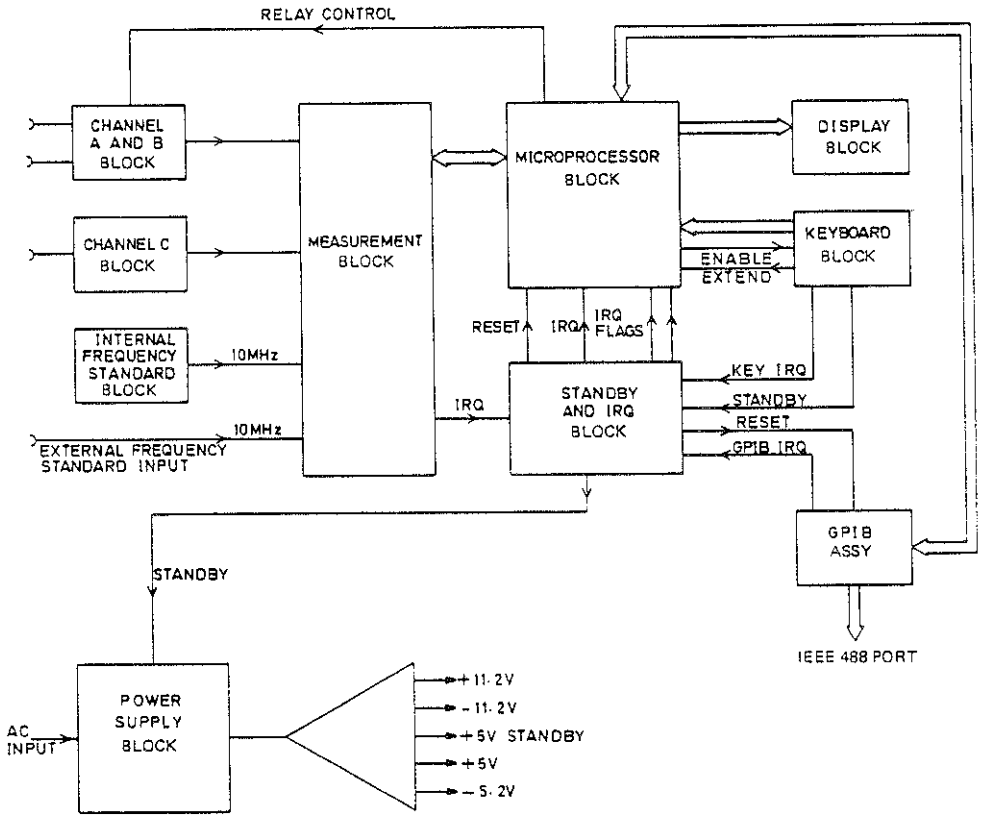


Figure 5.1 - Simplified Overall Block Diagram

5.3 THEORY OF OPERATION BY BLOCK

5.3.1 Channel A/B Block

5.3.1.1 Functional Description

5.3.1.1.1 Channel A/B block processes the signals applied at the respective A/B inputs to produce differential pairs of signals which are fed to the measurement block. A block diagram is shown in Figure 5.2.

5.3.1.1.2 Each channel includes relay-controlled circuits which allow selection of 50Ω /1MΩ input impedance, AC/DC coupling, and x1/x10 attenuation. The COM(mon) A configuration (Channel B signal disconnected and Channel A signal connected to both amplifiers in parallel) can be selected.

5.3.1.1.3 The channel amplifiers feature separate high frequency and low frequency paths. The crossover frequency is nominally 5 kHz. Signal filtering can be introduced, in Channel A only, by disconnecting the high-frequency amplifier path and increasing the bandwidth of the low frequency path to 50 kHz nominal. The signals from the high and low frequency paths are combined and drive a Schmitt trigger output stage.

5.3.1.1.4 The trigger levels for the two channels are derived independently in the digital-to-analog converter (DAC) using data supplied from the microprocessor.

5.3.1.1.5 Control signals for the system relays are supplied from the microprocessor.

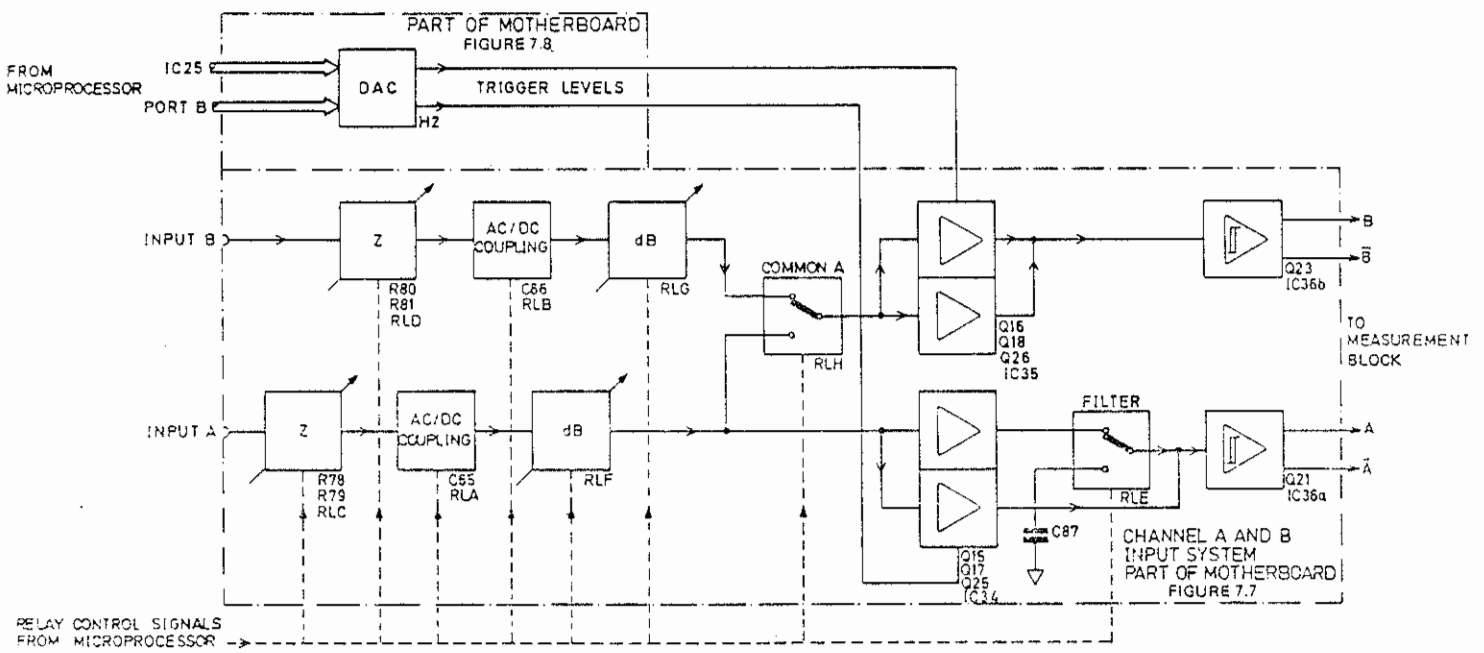


Figure 5.2 - Channel A/B Block Diagram

5.3.1.2 Circuit Description

5.3.1.2.1 Refer to the schematic shown in Figure 7.7. When relay RLC is energized, the input impedance seen at SK5 (INPUT A) is 50Ω , given by resistors R78 and R79 in parallel.

5.3.1.2.2 When energized, RLA gives DC coupling of the input signal. With RLA deenergized, the signal is AC coupled via C65. R165 limits the current surge which occurs if DC coupling is selected while C65 is in the charged state.

5.3.1.2.3 The x1/x10 attenuator is formed by R82, R83, R87 and RLF. With RLF deenergized, the attenuator has a series element, R82, and a shunt element formed by R83 and R87 in parallel. The attenuation is 20 dB (nominal). With RLF energized R82 is short-circuited, giving 0 dB attenuation.

5.3.1.2.4 The attenuator output is fed to the high-frequency channel buffer, Q15 and Q17, via R160 and C73. The gate of Q15 is protected against excessive negative voltage swings by D5. The gain from the attenuator output to the emitter of Q17 is approximately 0.94.

5.3.1.2.5 The buffer of the low frequency channel, IC34 and Q25, receives its input from the potential divider R87. The gain from R87 pin 1 to the emitter of Q25 is approximately 0.94. Any offset in the system can be nulled by adjusting R192.

5.3.1.2.6 When RLE is deenergized (Channel A filter not selected), the signals from the two buffers are combined at the base of Q21 by the network C79 and R107. These components act as a low-pass filter to the output of the low frequency buffer, and as a high-pass filter to the output of the high frequency buffer. The crossover frequency is 5 kHz.

5.3.1.2.7 The signal at Q21 emitter is fed to the Schmitt trigger IC36a via the diode bridge formed by D18, D19, D20, and D21. This protects the input of IC36a by limiting the signal swing to approximately ±1V.

5.3.1.2.8 The differential output of IC36 forms the input to the measuring block. The hysteresis of IC36, and therefore the channel sensitivity, can be set by adjusting R149.

5.3.1.2.9 The trigger level is set by the DAC, H2, shown in Figure 7.8 and is fed to IC34-2 via R202 and one section of R89. Feedback, taken from the emitter of Q21 to IC34-2 via R89 pins 5 and 3, makes R89 pin 3 a virtual ground point, and the gain from the R136/R202 junction to the emitter of Q21 is -0.94. A 1 VDC level at the Channel A input and a 1V trigger level, therefore, combine to give 0V at Q21's emitter. Thus, the selected trigger point on the input signal is always brought to 0V at Q21's emitter.

5.3.1.2.10 When Channel A's low-pass filter is selected, RLE is energized. This opens the high-frequency channel circuitry and connects C87 across the low frequency channel. The low-frequency channel bandwidth is then nominally 50 kHz.

5.3.1.2.11 The circuit of Channel B is similar to that of Channel A, but is not provided with a low-pass filter. Energizing RLH connects the signal applied at the Channel A input to both channel amplifiers.

5.3.1.2.12 The relays are controlled by the microprocessor. The voltage levels on the control lines are latched in IC24 as shown in Figure 7.8.

5.3.2 CHANNEL C BLOCK

5.3.2.1 Functional Description

5.3.2.1.1 Refer to the block diagram given in Figure 5.3. Channel C processes the signal applied at the Channel C input and feeds it to the measurement block.

5.3.2.1.2 Channel C's input is protected by a fuse, mounted in the input connector, and by a signal-limiting circuit. Next is an automatic level control circuit which reduces the range of the signal level applied to the amplifier.

5.3.2.1.3 After amplification, the signal is prescaled by 64 before being passed via a buffer and a signal gate to the measurement block.

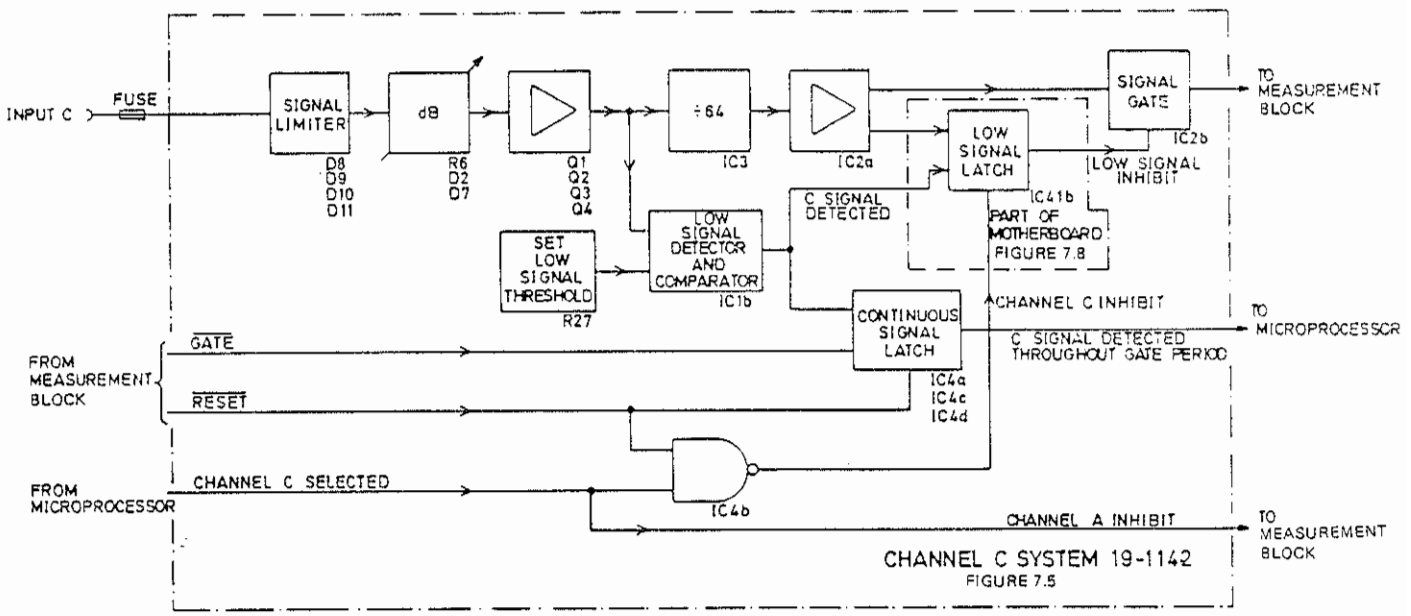


Figure 5.3 - Channel C Block Diagram

5.3.2.1.4 The amplitude of the signal at the amplifier output is monitored by a detector and comparator. The comparator output controls the low-signal latch. If the detector output is below the threshold, the latch is set and the channel output is inhibited by the signal gate. When the detector output goes above the threshold, the low-signal latch is armed and opens the signal gate on the next signal edge from the prescaler. This enables the instrument to make measurements on signal bursts.

5.3.2.1.5 The detector output is also applied to the continuous signal latch. This latch is reset at the beginning of each gate period and is set if the detector output falls below the threshold level. The microprocessor samples the latch output throughout the gate period. If the measured signal falls below the threshold level during this period, the measured result is set to zero.

5.3.2.1.6 If Channel C is not selected, the low-signal latch is held in reset by a control signal from the microprocessor and the output to the measurement block is inhibited. The same control signal is used to enable Channel A so that the two channels cannot be enabled at the same time.

5.3.2.2 Circuit Description

5.3.2.2.1 Refer to the schematic shown in Figure 7.5. The signal to be measured is connected via SK13 (INPUT C). The circuit is protected by a fuse which is mounted within SK13. The signal amplitude is limited by the diode clamp comprised of D8, D9, D10, and D11.

5.3.2.2.2 A degree of automatic gain control is achieved by means of an attenuator, formed by R6 and the impedance of the PIN diodes D2 and D7. The peak-to-peak detector D1, D3, R7, and C48 produces a negative voltage proportional to the signal amplitude. A direct current proportional to this voltage flows through the PIN diodes via L1. The impedance of the diodes decreases if the current increases so that changes in signal amplitude are offset by changes in attenuation.

5.3.2.2.3 The signal passes through four amplifier stages incorporating Q1, Q2, Q3, and Q4. The amplified signal is fed to the counter IC3 via the shaping circuit formed by R37, C46, and R36.

5.3.2.2.4 The signal frequency is prescaled by 64 in IC3 and buffered in IC2a. Provided that Channel C is selected and the amplitude of the signal is adequate, the output at IC2a-2 passes to the measurement block via the gate IC2b and SK7 pin 5.

5.3.2.2.5 The signal at the output of Q4 is fed to the low-signal detector D5 and C23. The comparator IC1b compares the detector output with a threshold voltage set by R27. The comparator output is at logic 1 if the detector output is below the threshold (Channel C's signal amplitude too low for accurate counting).

5.3.2.2.6 The logic level at the comparator output is inverted in IC1-A and is fed via SK7 pin 14 to the D input (pin 10) of the low-signal latch IC41b shown in Figure 7.8. IC41b is clocked by the output of IC2-A via SK7 pin 8. If the signal from Q4 is below the threshold, IC41b-14 goes to logic 1. This level is fed back via SK7 pin 7 to disable the gate IC2-B and inhibit the output to the measurement block.

5.3.2.2.7 The $\overline{\text{GATE}}$ signal enters the system at SK7 pin 17 and is inverted in IC1-C. The resulting signal and the output of the comparator IC1-B are fed to IC4-A. If both inputs are at a logic 1, indicating that the Channel C signal level is too low while the gate is open, the continuous signal latch IC4-C and IC4-D is set. The latch output is fed to the microprocessor via SK7 pin 11 and prevents the result of any measurement made during that gate period from being displayed.

5.3.2.2.8 The U signal at SK7 pin 16 is at a logic 1 when Channel C is selected. A buffered version of this signal is fed to SK7 pin 1 via IC2-C and disables Channel A at IC41a shown in Figure 7.8. When Channel C is not selected, SK7 pin 16 is at logic 0. This level is inverted and buffered in IC4-B and IC1-D, and is then fed to IC41b via SK7 pin 13. IC41b is held in reset, inhibiting the Channel C signal at IC2-B via SK7 pin 7.

5.3.3 Measurement Block

5.3.3.1 Functional Description

5.3.3.1.1 The measurement circuits of the instrument are provided by three custom-built integrated circuits. These are the two Multiple Counter and Control (MCC) circuits, MCC1 and MCC2, and the Timing Error Correction (TEC) circuit. A block diagram is shown in Figure 5.4.

5.3.3.1.2 The circuits within MCC1 and MCC2 are configured by the microprocessor according to the measurement function selected. The recipromatic counting technique is used. With this technique the measured signal, not the counter clock pulses, controls the start and stop of the measurement period (gate time) as shown in Figure 5.5. The gate time, therefore, extends over an integral number of cycles of the measured waveform. The gate time is measured by counting the clock pulses which occur while the gate is open. This leads to timing errors at both ends of the gate time, as shown. The TEC circuit enhances the measurement accuracy by compensating for these errors.

5.3.3.1.3 For all measurement functions except FREQ A and PERIOD A, the signals to be measured are fed directly to MCC2. For FREQ A and PERIOD A, the Channel A signal is scaled by two and fed to the $\overline{C}$ input of MCC2. When FREQ C is selected, the prescaler is disabled by the CHANNEL A INHIBIT signal from the Channel C block.

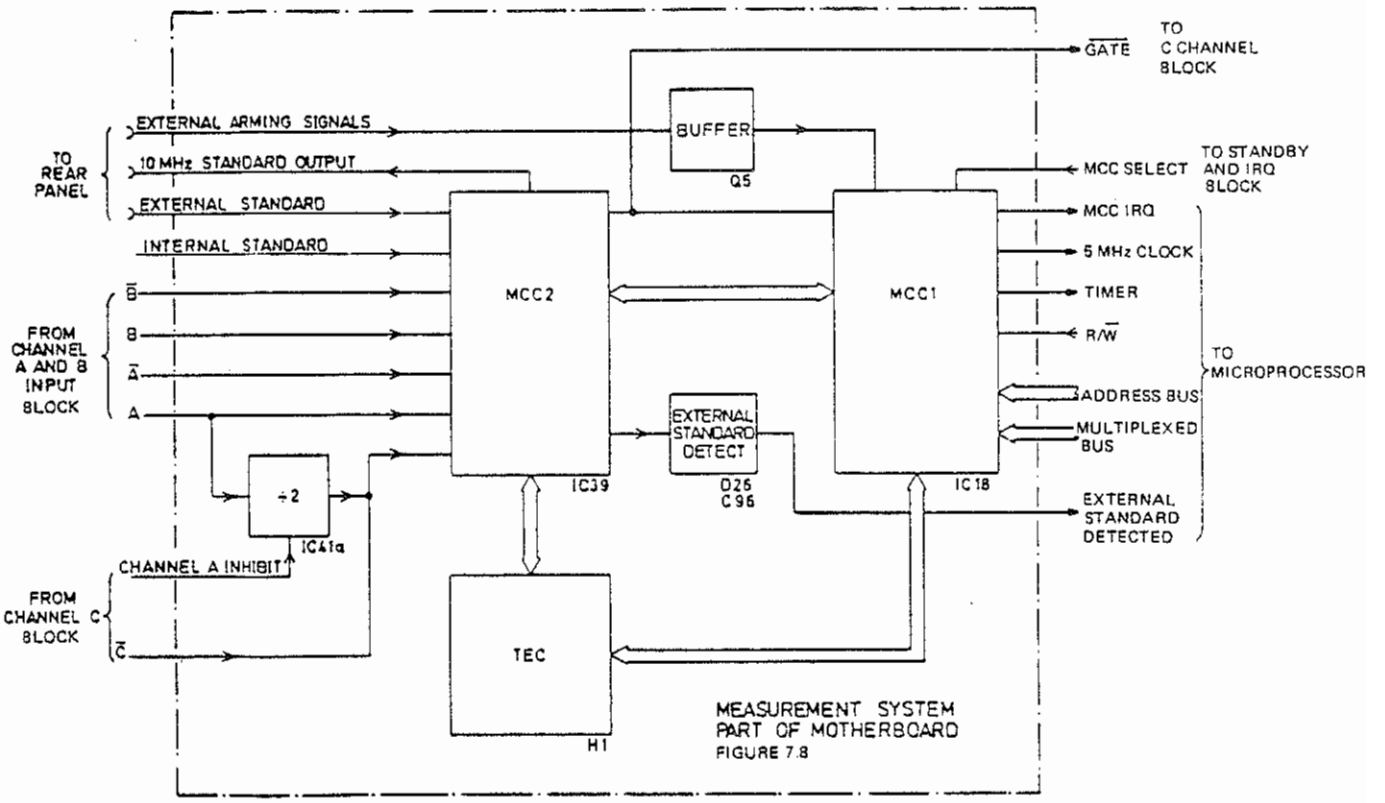


Figure 5.4 - Measurement - Block Diagram

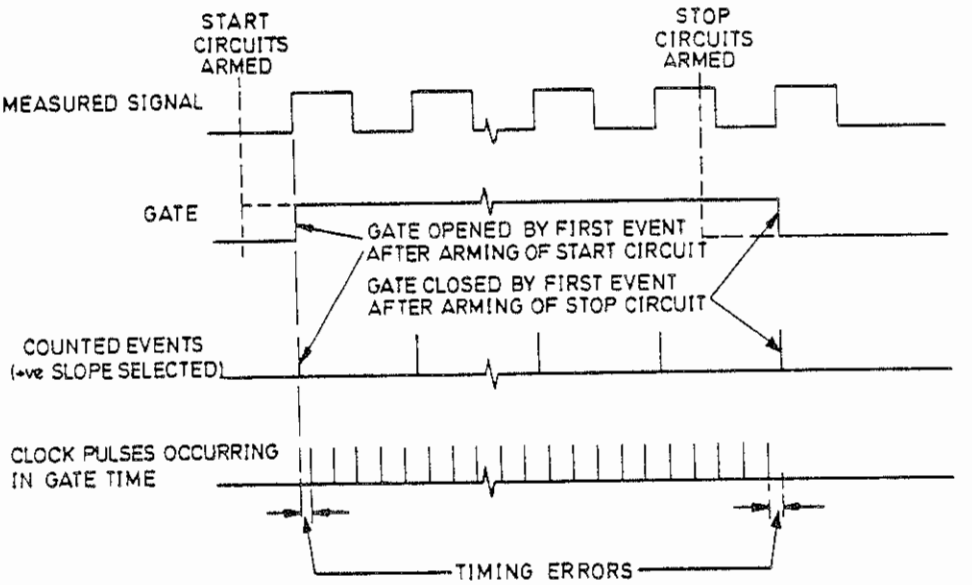


Figure 5.5 - Basic Reciprocatic Counting Technique

5.3.3.1.4 At the end of each measurement period, MCC1 generates an interrupt request for the microprocessor. The registers within MCC1 are addressed using the address bus and the MCC SELECT line. The measured value is transferred to the microprocessor via the multiplexed bus.

5.3.3.1.5 The internal and external frequency standard inputs are both fed to MCC2. The system will operate from the external standard provided that the input is of sufficient amplitude. A 10 MHz output, derived from the frequency standard in use, is made available at a socket on the rear panel.

5.3.3.2 Circuit Description

5.3.3.2.1 Refer the the schematic shown in Figure 7.8.

5.3.3.2.2 Measured Signal Input

5.3.3.2.2.1 For all measurement functions other than FREQ A and PERIOD A, the differential outputs from Channel A and Channel B are applied to the measuring circuit at IC39-15, 16, 17 and 18. For the FREQ A and PERIOD A functions, the A signal frequency is divided by two in IC41a and fed to IC39-19.

5.3.3.2.2.2 For the FREQ C and RATIO C/B functions, the $\overline{C}$ signal is fed to IC39-19. For these functions IC41a-5 is held at logic 1 by the PST1 control line (CHANNEL A INHIBIT) from the Channel C block. As a result, IC41a is held in set and the A signal is inhibited from reaching IC39-19.

5.3.3.2.3 Reference Frequency

5.3.3.2.3.1 The internal reference signal is applied to IC39-2 and the external reference signal, if present, to IC39-3. A buffered version of the external reference is present at IC39-24 and is applied to the detector D26, C96, and R129. The detector output is fed to IC23-6 and is read periodically by the microprocessor. If the level is above the TTL logic 1 threshold, the microprocessor sets IC39-38 to logic 0 and the measurement block switches to use the external reference.

5.3.3.2.3.2 A 10 MHz signal, derived from the frequency standard, is present at IC39-37 and is fed to the 10 MHz STD OUTPUT socket on the rear panel via PL19 pin 2.

5.3.3.2.3.3 A 10 MHz reference signal, derived from the frequency standard, is present at IC39-36. This signal is applied to the TEC, H1, at pin 6, and, after inversion in IC29e, to IC18-24.

5.3.3.2.4 Microprocessor Clock and Timer

5.3.3.2.4.1 A 5 MHz clock signal for the microprocessor (and the GPIB microprocessor if fitted) is taken from IC18-2. A 39.0625 kHz clock signal for the microprocessor timer is taken from IC18-4.

5.3.3.2.5 Channel C Gate and Reset

5.3.3.2.5.1 A $\overline{\text{GATE}}$ signal (logic 0 during the measurement period) and a $\overline{\text{RESET}}$ signal (negative-going pulse at the end of each measurement period) are taken from IC39-27 and IC18-40 and fed to the Channel C block via PL7 pins 17 and 15.

5.3.3.2.6 External Arming Input

5.3.3.2.6.1 Signal connected to the EXT ARM INPUT socket on the rear panel are fed to IC18-27 via PL19 pin 1 and the amplifier stage Q5.

5.3.3.2.7 Control Signals

5.3.3.2.7.1 The logic levels on lines Q0 to Q4, between IC18 and IC39 are shown in Table 5.1. These levels are stable if the following conditions exist:

a. No signals are applied to any of the channel inputs

b. Auto-trigger is disabled on Channels A and B

Table 5.1 - Control Logic Levels by Function

Measurement	Control Line				
Function:	QQ	Q1	Q2	Q3	Q4
FREQ A	1	1	0	1	0
PERIOD A	1	1	0	1	0
FREQ B	1	0	0	1	0
PERIOD B	1	0	0	1	0
FREQ C	1	1	0	1	0
T.I. A→B	0	0	1	1	0
T.I. B→A	0	0	0	1	0
TOTAL A by B	1	0	0	1	1
TOTAL B by A	1	0	1	1	1
RATIO C/B	1	1	0	1	1
RATIO A/B	1	0	1	1	1
Special Function 72	1	1	1	0	1
Special Function 73	1	1	1	0	0
Special Function 74	1	1	1	0	1
Special Function 75	1	1	1	0	0

NOTES:

a. The FREQ B, PERIOD B, TOTAL B by A, and T.I. B→A functions are obtained using Special Function 21.

b. Special Functions 72 to 75 can only be used when CHECK is selected.

5.3.4 Display Block

5.3.4.1 Functional Description

5.3.4.1.1 A simplified diagram of the display block is given in Figure 5.6. The GPIB LEDs, GATE LED, Channels A and B TRIGGER LEDs, and the STANDBY LED are held on or off by control signals from other systems. The remainder of the display is multiplexed under the control of the display drivers.

5.3.4.1.2 To update the display, the microprocessor selects the appropriate display driver using the MODE 1 and MODE 2 control lines. A string of nine 8-bit words (a control word and eight data words) is then put onto the bus. Each word is entered into a memory within the display driver under the control of the STROBE signal.

5.3.4.1.3 The display driver then sequentially puts the data words onto its output bus. For each data word, the appropriate numeric indicator or group of LEDs is enabled by a signal on its control line.

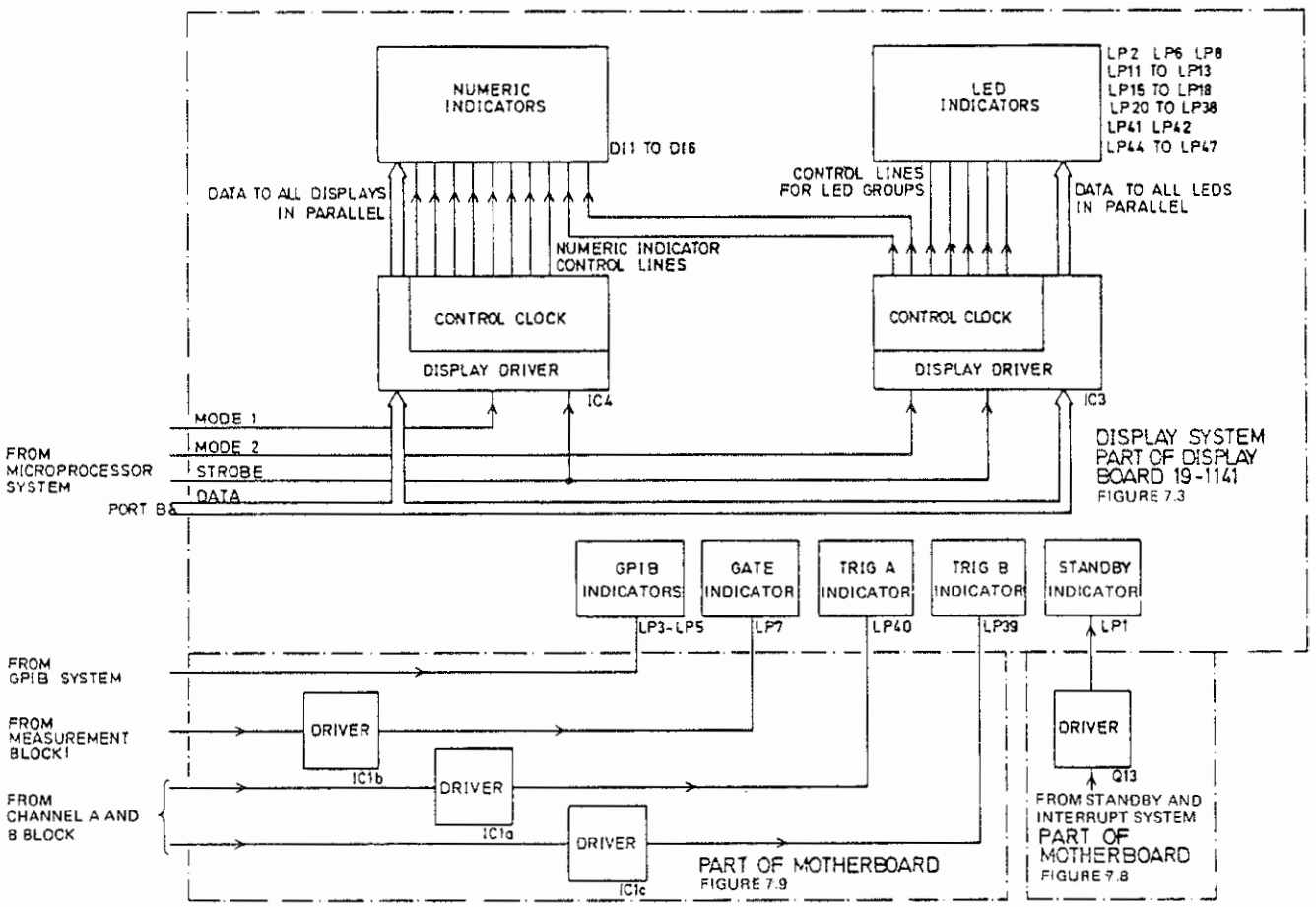


Figure 5.6 - Display-Block Diagram

5.3.4.2 Circuit Description

5.3.4.2.1 The schematic is shown in Figure 7.3. The GPIB LEDs LP3, LP4, and LP5 are driven via SK1 from the GPIB system. The GATE LED LP7 is driven from the measurement block via a driver stage, shown in Figure 7.9, and SK2 pin 11. The TRIG LEDs LP39 and LP40 are driven from the Channel A/B block via driver stages, shown in Figure 7.9, and SK2 pins 7 and 3. The STANDBY LED LP1 is driven via SK1 pin 8 from the standby and interrupt block. The remaining LED indicators and the numeric indicators DI5 and DI6 are controlled by the display driver IC3. Numeric indicators DI1 to DI4 are controlled by IC4.

5.3.4.2.2 Display data is stored in memory within IC3 and IC4. To change the data, the microprocessor puts a control word on the port B bus. The microprocessor writes this word into the display driver by means of a negative pulse applied to the DISPLAY STROBE line at SK1 pin 4. The control word determines the operating mode of the display drivers.

5.3.4.2.3 The microprocessor then selects the display driver required by setting a logic 0 on the appropriate MODE line at SK1 pin 3 or 6. Eight words containing display data are written into the selected display driver via the port B bus, controlled by eight negative-going pulses on the DISPLAY STROBE line.

5.3.4.2.4 The output of each display driver is multiplexed under the control of an internal clock. Eight-bit display data (for seven segments + decimal point or eight LED indicators) are put onto the device output bus (pins 1 to 4 and 24 to 27). A positive pulse is then applied to the enablement line of the device or group of indicators which is to display the data. The enablement line waveforms consist of 500 μs positive-going pulses at approximately 250 pps.

5.3.5 Keyboard Block

5.3.5.1 Functional Description

5.3.5.1.1 A simplified diagram of the keyboard block is given in Figure 5.7. The encoding of the keyboard data is performed within the system without microprocessor action. An interrupt request (IRQ) is made to the microprocessor when encoding is complete. Data transfer is initiated by the KEYBOARD ENABLE signal from the microprocessor.

5.3.5.1.2 The 32 keys are divided into two 16-key matrices. When a key is pressed, its position is encoded into a 5-bit word. One bit, carried on the $\overline{\text{KEYBOARD EXTEND}}$ line, indicates the matrix in which the key is located. The remaining bits indicate the position of the key within the matrix.

5.3.5.1.3 When a key is pressed, the encoder examines both matrices simultaneously and generates a 4-bit code representing the key position. The same four bits are generated regardless of the matrix in which the key is located.

5.3.5.1.4 If the key pressed is in the extended key matrix, one of the inputs to the NAND gate is pulled low. The $\overline{\text{KEYBOARD EXTEND}}$ line is then set to logic 0. If the key is in the non-extended matrix, the inputs to the NAND gate are isolated from the key line by one of the diodes and the $\overline{\text{KEYBOARD EXTEND}}$ line remains at logic 1.

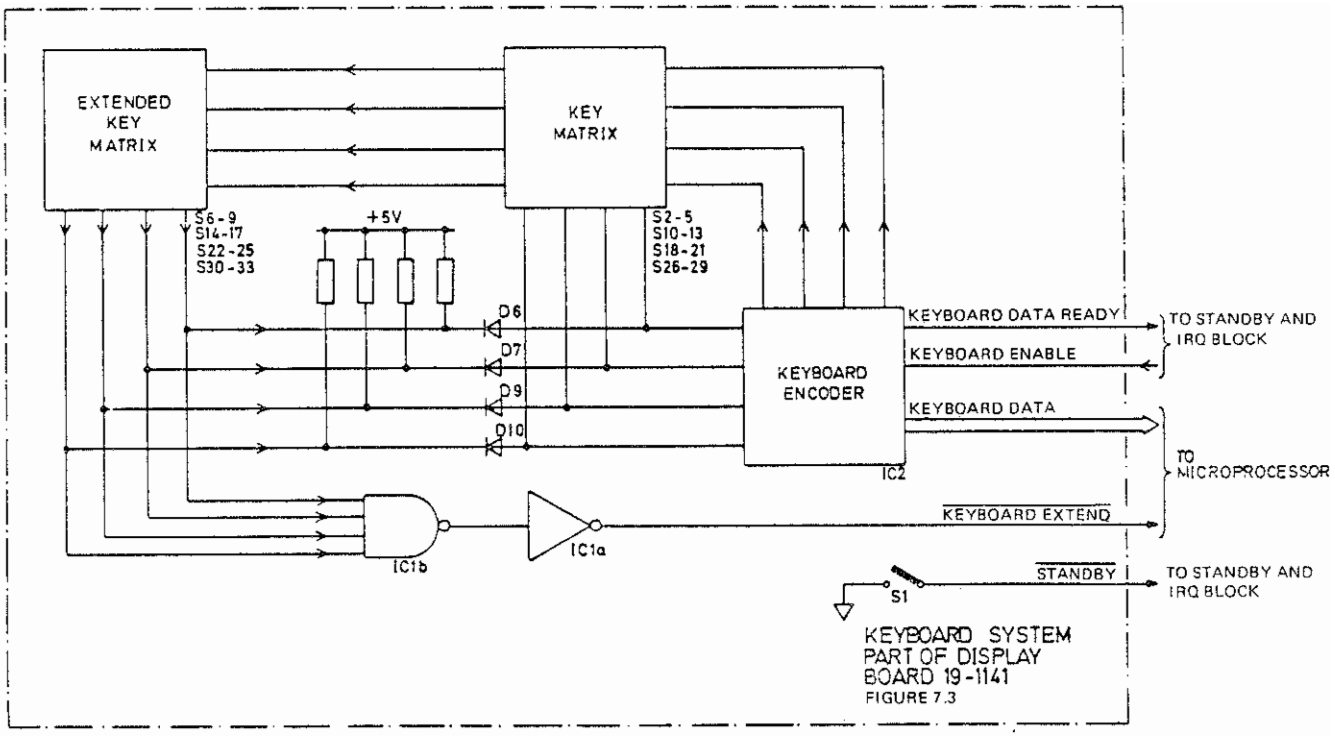


Figure 5.7 - Keyboard-Block Diagram

5.3.5.2 Circuit Description

5.3.5.2.1 The schematic is given in Figure 7.3. The keys are divided into two 16-key matrices having common row lines connected to the encoder at IC2-7, 8, 10, and 11. The matrices have separate column lines connected in pairs to IC2-1, 2, 3, and 4.

5.3.5.2.2 The encoder normally holds the row lines at logic 0. When a key is pressed, the corresponding column line is pulled to logic 0. The encoder then scans the keyboard and stores a 4-bit code, corresponding to the row and column of the key, in an internal register. Because the column lines are connected to the encoder in pairs, it cannot find which matrix contains the key.

5.3.5.2.3 The $\overline{\text{KEYBOARD EXTEND}}$ line indicates which matrix contains the key that is pressed. The inputs to IC2 are normally held at logic 1 so that SK2 pin 9 is at logic 1. If a key in the extended matrix (column lines connected directly to the inputs of IC1b) is pressed, one input of IC1b is pulled to logic 0 and SK2 pin 9 will go to logic 0. The column lines of the other matrix are isolated from the inputs of IC2 by D6, D7, D9, and D10, so that the logic level at SK2 pin 9 is not changed when a key in this matrix is pressed.

5.3.5.2.4 When the key-position code has been stored, the encoder sets the KEYBOARD DATA READY line, at SK2 pin 4, to logic 1 giving a microprocessor interrupt. The microprocessor sets IC2-13 to logic 0 using the $\overline{\text{KEYBOARD ENABLE}}$ line, and the encoder puts the 4-bit code onto the bus. The microprocessor reads the code and the state of the $\overline{\text{KEYBOARD EXTEND}}$ line to determine which key has been pressed.

5.3.6 Microprocessor Block

5.3.6.1 Functional Description

5.3.6.1.1 A simplified diagram of the microprocessor block is given in Figure 5.8. The microprocessor used has a 5-bit bus for the high-order address bits and an 8-bit multiplexed bus which is used for the low-order address bits and for data. The low-order address bits are strobed into the address latch, which holds them on an 8-bit address bus, to free the multiplexed bus for data.

5.3.6.1.2 Two latches, fed from port B of the microprocessor, are used to maintain voltage levels on the instrument control lines. A third latch is used to read the status of the instrument flags via port B. The latches and registers for the connection of the multiplexed bus to the measurement system are in the measurement block, and are controlled by the MCC SELECT signal. The display data latches are in the display block, and are controlled by strobe and chip select signals obtained from port A.

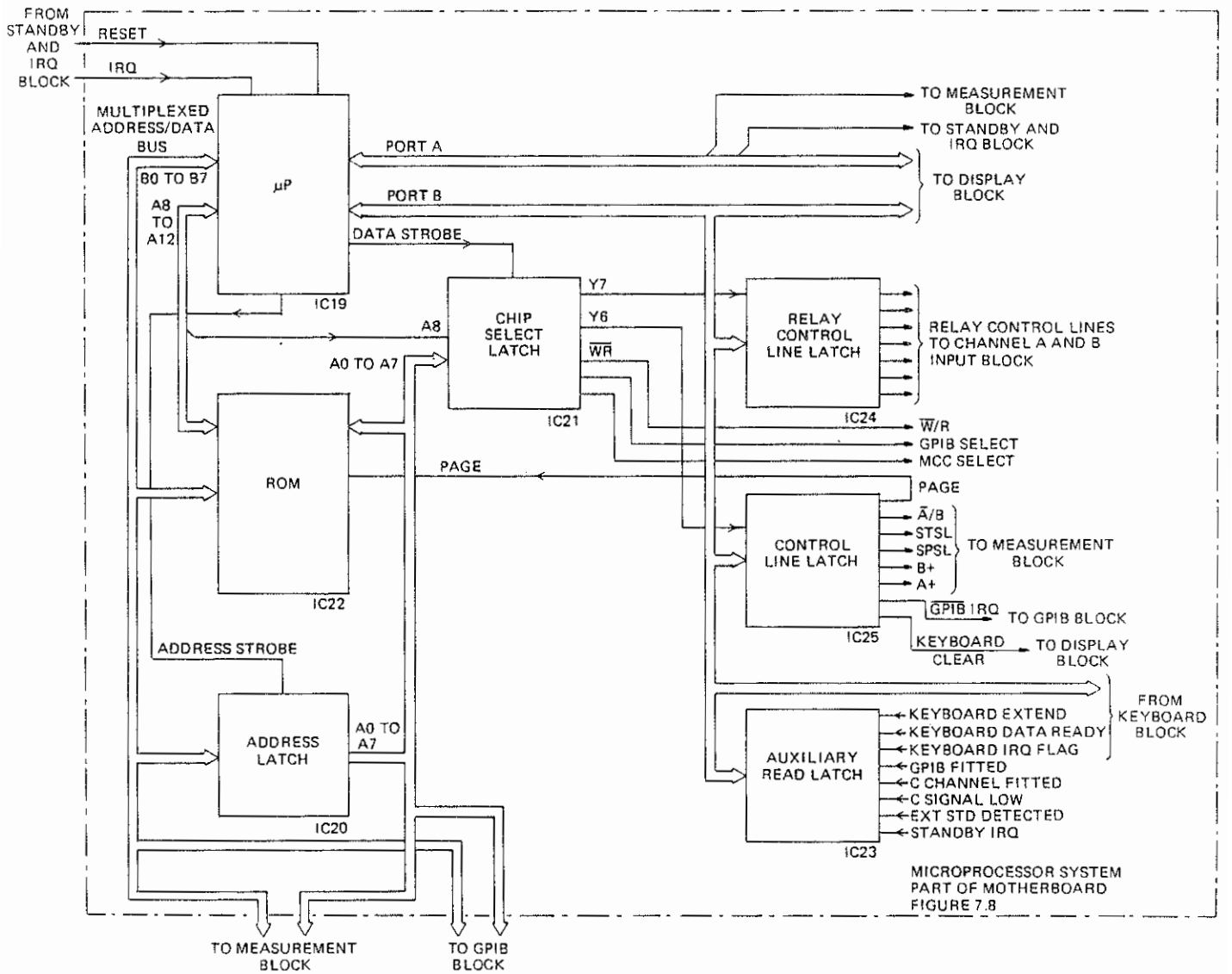


Figure 5.8 - Microprocessor-Block Diagram

5.3.6.2 Circuit Description

5.3.6.2.1 The schematic is given in Figure 7.8. The microprocessor clock and timer signals are generated in the measurement block and are fed to IC19-39 and IC19-37. A $\overline{\text{RESET}}$ signal is generated in the standby and IRQ block when the instrument is switched on or off and is fed to IC19-1.

5.3.6.2.2 The microprocessor bus for the high-order address bits is designated A8 to A12. The multiplexed bus, used for the low-order address bits and for data is designated B0 to B7. The microprocessor also has two input/output ports PA0 to PA7 and PB0 to PB7.

5.3.6.2.3 Multiplexed Bus Operation

5.3.6.2.3.1 The microprocessor puts IC19-6 (ADDRESS STROBE) at logic 1 and (DATA STROBE) at logic 0. This enables the address latch IC20 (IC20-11 at logic 1), disables ROM IC22 (IC22-20 at logic 1), and disables the address decoder IC21 (IC21-6) at logic 0).

5.3.6.2.3.2 This address is put onto lines B0 to B7 and A8 to A12. When the lines have settled, the ADDRESS STROBE line is taken to logic 0. The low-order bits of the address are latched into IC20 and are held on address lines A0 to A7. Lines B0 to B7 are now free for use as a data bus.

5.3.6.2.4 Address Decoding

5.3.6.2.4.1 The levels on address lines A6 to A12 are decoded in IC21 to provide the following outputs:

a. $\overline{\text{MCC SEL}}$, the chip-select signal for IC18

b. $\overline{\text{GPIB SEL}}$, the chip-select for the GPIB address decoder

c. $\overline{\text{WR}}$, the write control signal for H2

d. Y6, the chip select signal for output latch IC25

e. Y7, the chip select signal for output latch IC24

5.3.6.2.4.2 These outputs are only available when IC21 is enabled by a logic 1 at IC21-6 and a logic 0 at IC21-4,5. The level at IC21-6 is set by the DATA STROBE output at IC19-4, which is at logic 1 when the multiplexed bus is available for data transfer. All outputs from IC21 are decoded from addresses with lines A9 to A12 at logic 0 when IC21-4, 5 are held at logic 0 by the output from IC27a, b, and d.

5.3.6.2.5 Input and Output Latches

5.3.6.2.5.1 The logic levels required on the instrument control lines and on the PAGE line (most significant bit of RAM address) are set into the output latches IC24 and IC25 from data port B of the microprocessor. The latch strobe signals are decoded in IC21. Data may be read by the microprocessor from the input latch IC23. The latch strobe signal is provided via data port A of the microprocessor.

5.3.7 Standby and IRQ Block

5.3.7.1 Functional Description

5.3.7.1.1 This block generates reset signals for the microprocessor and GPIB interface, and the standby switching signal for the power supply system. It also combines the IRQ signals from the GPIB interface, the measurement block, and the keyboard block for connection to the microprocessor. A block diagram is given in Figure 5.9.

5.3.7.1.2 Reset signals for the microprocessor and the GPIB interface are generated whenever power is applied to or removed from the instrument's power supply system.

5.3.7.1.3 On switching to standby, the standby signal from the keyboard block sets the standby IRQ latch. The latch outputs provide the standby IRQ and a standby flag for the microprocessor. The standby IRQ output also clocks the standby ON/OFF latch to the set state. This provides signals to switch the power supply to standby, light the STANDBY LED, and disable IC30b, thereby inhibiting the other IRQs. At the end of the microprocessor interrupt routine, the standby IRQ latch is reset, removing the standby IRQ. The state of the standby ON/OFF latch is not changed.

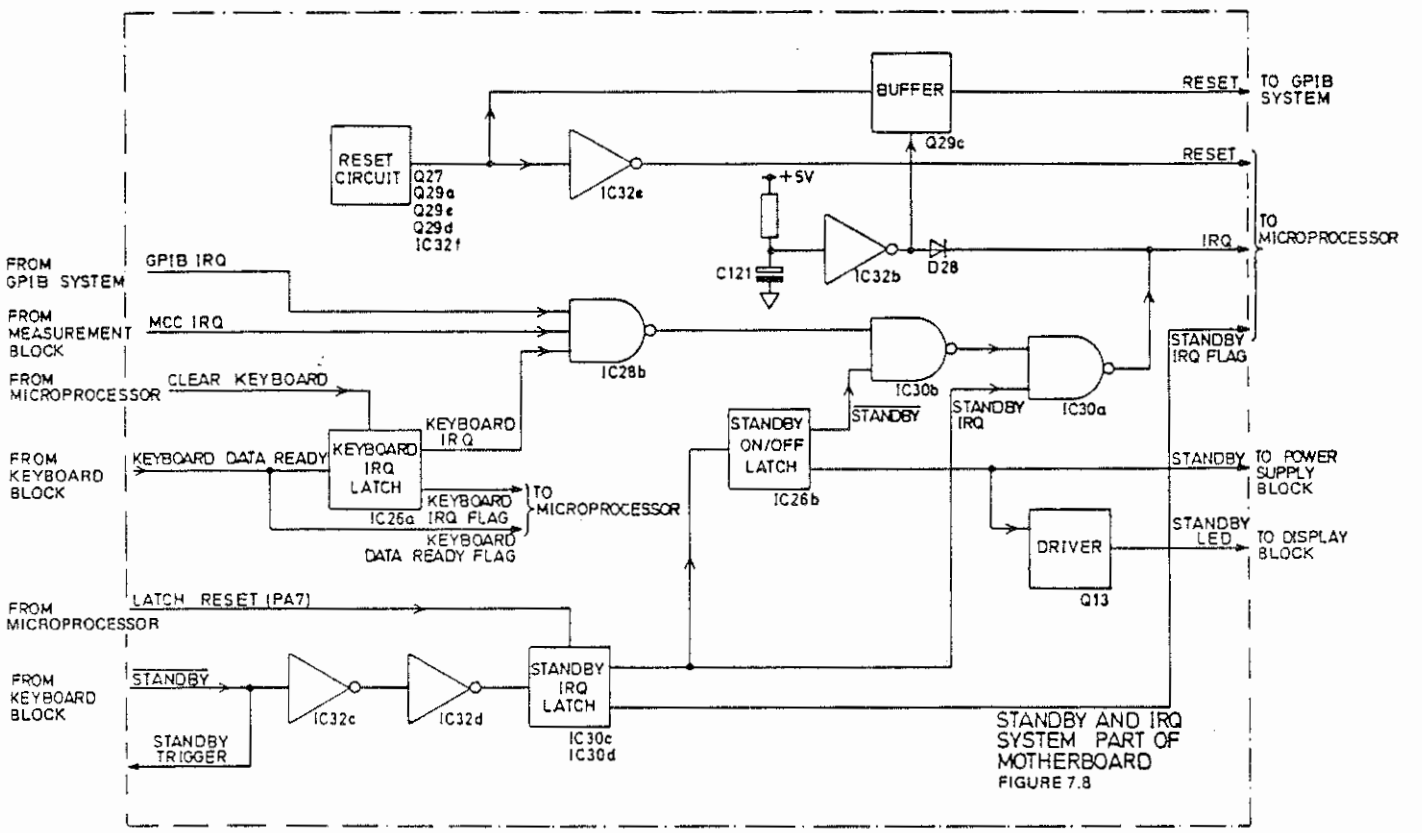


Figure 5.9 - Standby and IRQ Block Diagram

5.3.7.1.4 While the instrument is in standby, the input to IC32b is held low and the IRQ input to the microprocessor is held high via D28. This inhibits all IRQs. The output from IC32b also holds the GPIB interface in reset via Q29c.

5.3.7.1.5 On return from standby, the standby IRQ latch is again set by the standby signal from the keyboard block. The standby ON/OFF latch is clocked to the reset state, the power supply is returned to normal operation, and IC30b is enabled. The input to IC32b rises as C121 charges, removing the reset signal from the GPIB interface and enabling the microprocessor IRQ input. The microprocessor is now able to accept the IRQ from IC30a. At the end of the restart sequence, the standby IRQ latch is reset.

5.3.7.1.6 When the encoder in the keyboard system has data ready to be read by the microprocessor, the keyboard IRQ latch is clocked via the KEYBOARD DATA READY line. The latch outputs provide the keyboard IRQ and a keyboard IRQ flag. Once the keyboard has been identified as the source of the interrupt, the latch is reset by the microprocessor.

5.3.7.2 Circuit Description

5.3.7.2.1 The schematic is shown in Figure 7.8.

5.3.7.2.2 Reset Circuit

5.3.7.2.2.1 The $\overline{\text{RESET}}$ signal is generated in the circuit containing Q27, Q29a, d, and e, and C125. When the instrument is switched on, the input to IC32f is held low until C125 charges through R215, Q29a, and R216. The output at IC32f-12 goes to logic 1 when power is applied, but drops to logic 0 after approximately 500 ms. This output is inverted by IC32e to provide the microprocessor reset and by Q29c to provide the GPIB reset.

5.3.7.2.2.2 If there is a reduction in the +5V STANDBY supply, due to the instrument being switched off or to power failure, the potential across R217 falls. The potential at Q27 emitter is maintained by the charge in C125, so Q27 conducts. The current in R218 makes the base of Q29d positive, so the transistor conducts and holds the base of Q27 low until C125 is completely discharged. This ensures that a good reset action is obtained, even if the power is quickly restored.

5.3.7.2.3 Standby Operation

5.3.7.2.3.1 On switching to standby, PL1 pin 14 is taken to 0V by the STANDBY key. Debouncing is provided by R158 and C126. The leading edge of the signal is sharpened in IC32c, C118, R151, and IC32d, and sets the standby IRQ latch IC30c, d.

5.3.7.2.3.2 The negative-going output from IC30c-10 is passed via IC30a, IC32a, and R152 to IC19-2 to provide a microprocessor interrupt. The positive-going output from IC30d-11 forms the standby IRQ flag (read by the microprocessor via IC23 during the interrupt routine) and clocks the standby latch IC26b to the set state.

5.3.7.2.3.3 The logic 0 level at IC26b-8 switches on Q13 and provides power for the STANDBY LED via PL1 pin 8. The same output is applied to IC30b-5 and disables the other interrupts which are connected to IC30b-6.

5.3.7.2.3.4 The logic 1 level at IC26b-9 shuts down the power supplies except the +5V STANDBY supply.

5.3.7.2.3.5 At the end of the interrupt routine, the microprocessor resets the standby IRQ latch by applying logic 1 to IC30c-8 from IC19-7.

5.3.7.2.3.6 On return from standby, the standby IRQ latch is again set. This provides a microprocessor interrupt and sets the standby IRQ flag as before. The positive-going output from IC30d-11 clocks the standby latch back to the reset state, so that the STANDBY LED is turned off and the power supplies are restored. The microprocessor resets the standby IRQ latch at the end of the interrupt routine.

5.3.7.2.4 The IRQ Circuits

5.3.7.2.4.1 The KEYBOARD DATA READY line at PL2 pin 4 goes to logic 1 when the keyboard encoder has data available. This clocks IC26a to the set state to provide a keyboard IRQ flag at IC23-11 and an interrupt signal at IC28b-9. Interrupts from the measurement system ($\overline{\text{MCC IRQ}}$) and the GPIB interface ($\overline{\text{GPIBIRQ}}$) are connected to IC28b-12 and IC28b-10, 13.

5.3.7.2.4.2 If any of these interrupts occur, IC28b-8 and IC30b-6 will go to logic 1. Provided the standby latch IC26b is not set, IC30b-5 will be at logic 1 and the interrupt signal passes via IC30a and IC32a to IC19-2.

5.3.7.2.4.3 When the instrument is switched into or out of the standby state, the standby IRQ latch IC30c, d is set. The standby IRQ from IC30c-10 is fed to IC19-2 via IC30a and IC32a.

5.3.7.2.4.4 The circuit comprising R220, C121, IC32b, and D28 disables the microprocessor interrupt input and holds the GPIB microprocessor reset line low (via Q29c), while the +5V power supply to R220 is switched off. On return from standby, C121 charges and IC32b-4 goes to logic 0. The microprocessor interrupt input is enabled and the GPIB microprocessor is reset. The delay in enabling the interrupts prevents the standby IRQ, which occurs on return from standby, from being acted upon before the power supplies are fully restored.

5.3.8 Power Supply Block

5.3.8.1 Functional Description

5.3.8.1.1 A simplified diagram of the power supply block is given in Figure 5.10. The AC supply enters at a plug mounted on the rear panel and passes via a fuse and RFI filter, mounted on the motherboard, to the line switch.

5.3.8.1.2 The switched supply is connected to the primary winding of the power transformer via the operating-voltage range selector. The voltage range selector is a small plug-in printed circuit board which is positioned according to the desired line voltage.

5.3.8.1.3 The transformer has a tapped secondary winding which supplies two bridge rectifiers. The smoothed but unregulated outputs from the rectifiers feed regulators providing +11.2V, -11.2V, +5V, +5V and -5.2V. The -5.2V regulator and one of the +5V regulators, which supply most of the instrument's circuits, are shut down by a signal from the microprocessor when the instrument is switched to standby.

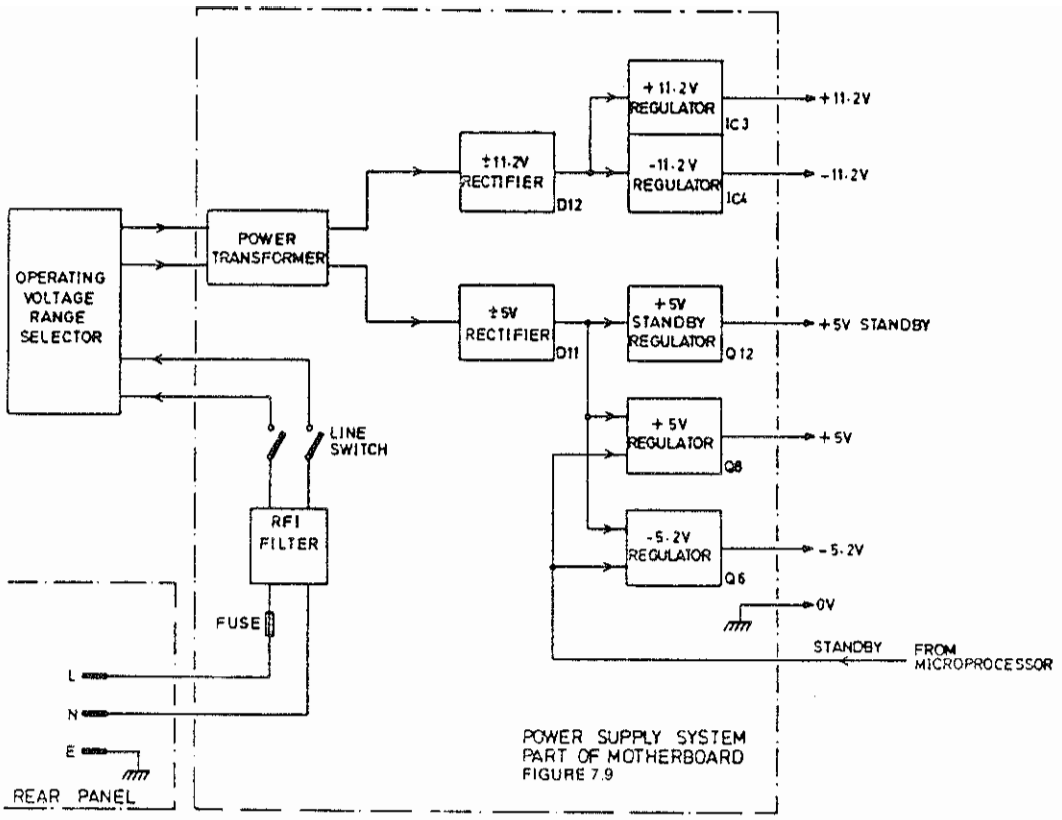


Figure 5.10 - Power-Supply-Block Diagram

5.3.8.2 Circuit Description

5.3.8.2.1 The schematic is shown in Figure 7.9. AC power connected at the power input plug passes via fuse FS1 and the RF filter, formed by L1, L2, C46, C47, and C48, to the POWER switch S1b. The switched supply is connected to the primary windings of transformer T1 via the tracks of a printed circuit board which is inserted in SK8.

5.3.8.2.2 The secondary windings fo transformer T1 suppy the ±5V rectifier D11, C49 and C50, and the ±11V rectifier D12, C52, and C59.

5.3.8.2.3 Regulated supplies at ±11.2V are provided by the regulators IC3 and IC4. The common terminals of these regulators are held at approximately -0.7V and +0.7V by diodes D13 and D14.

5.3.8.2.4 Regulated supplies at +5V are provided by two discrete component regulators having series elements Q8 and Q12. The non-inverting inputs to the comparators IC31a and IC31c are connected to a +2.5V reference voltage, derived in the hybrid circuit H2 shown in Figure 7.8. Potential dividers formed by elements of R49 hold each inverting input at half the output voltage of the associated regulator.

5.3.8.2.5 A regulated supply at -5.2V is provided by a discrete component regulator having Q6 as its series element. The comparator inputs are held at approximately 0V. The potential divider controlling the inverting input is connected across the +5V and -5.2V supplies.

5.3.8.2.6 Standby Mode

5.3.8.2.6.1 When the instrument is switched to standby, the standby latch IC26b (see Figure 7.8) is clocked to the set state. The base of Q11 is pulled high and IC31a-3 is pulled low. The base of Q9 is pulled low by IC31a, the base current of Q8 is cut off, and the regulator is shut down. When the voltage of the +5V supply falls, IC31b-6 goes more negative. The base of Q7 is taken towards 0V by IC31b so that the base current of Q6 is cut off and the -5.2V regulator is shut down.

5.3.9 Internal Frequency Standard Block

5.3.9.1 Functional Description

5.3.9.1.1 The internal frequency standard consists of a 5 MHz oscillator and a frequency doubler. A block diagram of the internal frequency standard is shown in Figure 5.11.

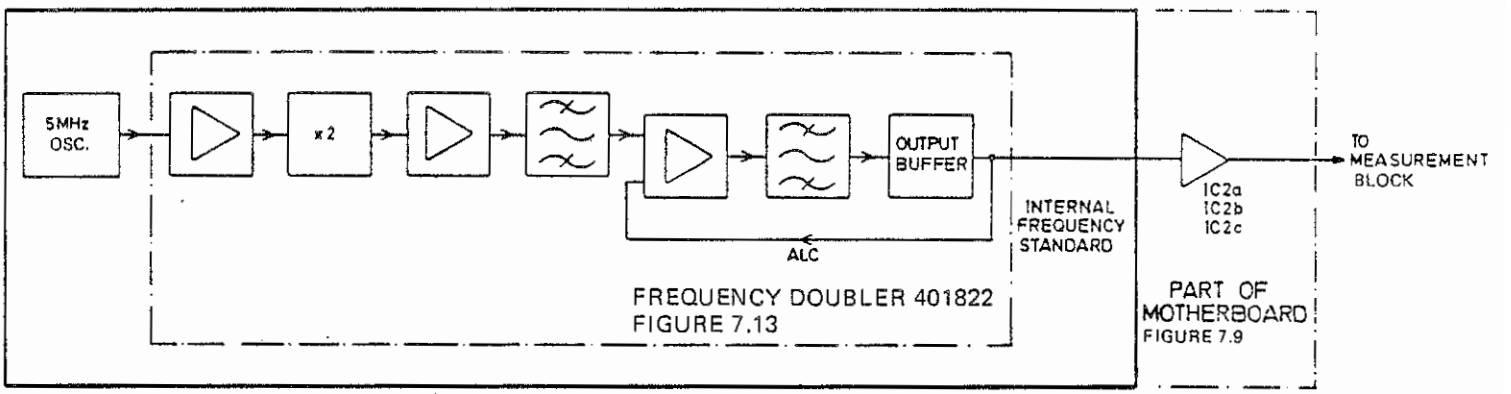


Figure 5.11 - Internal Frequency Standard Block Diagram

5.3.9.1.2 The 10 MHz signal is passed to the measurement block via a buffer (IC2) on the motherboard.

5.3.9.1.3 Signals from an external frequency standard are applied to a signal conditioning circuit on the motherboard. If a 10 MHz external frequency standard is used, the output of this circuit is connected directly to the measurement circuitry.

5.3.9.2 Circuit Description

5.3.9.2.1 Frequency Doubler

5.3.9.2.1.1 The schematic of the frequency doubler, used with the internal frequency standard is given in Figure 7.14. The 5 MHz input is applied to the balanced amplifier containing Q1 and Q2. The base of Q3 is driven by the differential outputs from the amplifier via D1 and D2 so that the frequency here is 10 MHz.

5.3.9.2.1.2 The 10 MHz signal is amplified and filtered in the two stages containing Q3 and Q5, and fed to pin 3 via buffer Q6.

5.3.9.2.1.3 The output signal is fed back via C6 to switch Q4 on during the positive peaks of the signal. The gain of Q5 is controlled by the potential across C3 which charges via R12 and discharges via Q4. If the output signal increases, the time for which Q4 conducts increases so that the mean potential across C3 decreases. The resulting decrease in gain of Q5 provides automatic level control.

5.3.9.2.2 Internal Frequency Standard Buffer

5.3.9.2.2.1 The buffer circuit is shown in Figure 7.9. The 10 MHz input at PL14 pin 4 is shaped and buffered in IC2a, IC2b, and IC2c before being fed to the measurement block at IC39-2. The inverting inputs of IC2 are connected to the bias voltage at IC2-11.

5.3.9.2.3 External Frequency Standard Buffer

5.3.9.2.3.1 The buffer circuit is shown in Figure 7.9. The signal connected to the EXT. STD. INPUT socket on the rear panel is fed to PL20 pin 4. Protection against excessive signal amplitude is provided by D6, D7, and R32.

5.3.9.2.3.2 The buffer comprises IC14a, IC14b, and IC14c. The inverting inputs are connected to the bias voltage at IC14-11. The final stage has feedback connected via R11 to give a Schmitt trigger action.

5.3.9.2.3.3 Link LK1 is fitted between pins 8 and 9 of the PL16 to connect the differential output of the final stage to the measurement block at IC39-3.

5.3.10 GPIB Interface

5.3.10.1 Introduction

5.3.10.1.1 The GPIB interface is a self-contained, microprocessor-controlled system. It handles the transfer of data between its internal memory and the GPIB without involving the main instrument's microprocessor. Data transfer is made one byte at a time, each transfer being controlled by the IEEE-488 handshake protocol. Refer to the schematic in Figure 7.11.

5.3.10.1.2 The microprocessor $\overline{\text{RESET}}$ signal is derived from the standby and IRQ block. The clock signal is derived from MCC1, IC18, shown in Figure 7.8.

5.3.10.1.3 The microprocessor uses a multiplexed bus, the eight low-order bits being used for both address and data. The low-order address bits are put onto the bus first and are latched into IC11 by the address strobe. The bus is then free for data use.

5.3.10.1.4 Data transfer between the microprocessors is initiated by an interrupt and is controlled by a 3-wire handshake protocol. The transfer is in the form of a data string, the number of bytes in the string being indicated by the first byte.

5.3.10.2 Address Setting and Recognition

5.3.10.2.1 The microprocessor reads the settings of the address switches in switchbank S1, via its port B inputs, approximately every 1 ms and writes the settings into an address register within the general purpose interface adapter (GPIA) IC12.

5.3.10.2.2 When the interface address is set on the bus by the controller, it is recognized by the GPIA by comparison with the contents of the internal address register.

5.3.10.3 Reading from the Bus

5.3.10.3.1 When the interface is addressed to listen, the GPIA conducts the handshake procedure up to the point where the ready for data (RFD) indication is given. At this point IC12-27 is at logic 0, giving a logic 1 level at IC18-11. This puts three of the bilateral switches of IC13 into the conducting state, thus completing the RFD line. The logic 0 at IC12-27 also puts the buffers in IC14 and IC15 into the receive condition. Data from the bus enters the GPIA data-in register and IC12-40 goes to logic 0 providing an interrupt request to the microprocessor IC9.

5.3.10.3.2 The microprocessor interrupt routine establishes the reason for the interrupt. The address decoder IC8 is enabled via IC27-15, IC26-8, and A7. The decoder is addressed using lines GA4, 5, and 6, and gives the GPIA enable signal at IC8-15. The data-in register of the GPIA is addressed using the R/$\overline{W}$ line and lines A0, 1, and 2. The microprocessor then reads the contents of the data-in register and transfers the data to memory.

5.3.10.3.3 When the data-in register has been read, the GPIA cancels the interrupt request and allows the data accepted (DAC) line to go high. The handshake routine then continues, and a further byte, if available is loaded into the data-in register. The interrupt and data transfer sequence is then repeated.

5.3.10.4 Writing to the Bus

5.3.10.4.1 When the GPIA is addressed to talk, its internal data-out register will normally be empty. Under these conditions IC12-40 goes to logic 0 and provides an interrupt request to the microprocessor.

5.3.10.4.2 IC17B is in the reset state, giving a logic 1 at IC18-12. Since IC12-27 is at logic 1 when the GPIA is addressed to talk, IC18-13 is also at logic 1. The resulting logic 0 at IC18-11 opens three circuits of bilateral switches in IC13 to break the RFD line. The fourth bilateral switch conducts, due to the logic 1 at IC19-10, and holds IC12-18 at 0V. Even if the listening device asserts that it is ready for data, IC12 will not attempt to load the contents of the data-out register onto the bus.

5.3.10.4.3 The microprocessor interrupt routine establishes the reason for the interrupt. The microprocessor then enables the address decoder, IC8, via IC27-15, IC26-8, and A7. The decoder is addressed using lines GA4, 5, and 6, and gives the GPIA enable signal at IC8-15. The data-out register of the GPIA is addressed using the R/$\overline{W}$ line and lines GA0, 1 and 2, and a data byte is written into the register. The GPIA then cancels the interrupt request.

5.3.10.4.4 Following the data transfer, the microprocessor sets IC17B, using line PB7, to give a logic 0 at IC18-12. This gives a logic 1 at IC18-11, which enables three bilateral switches in IC13 and connects the RFD line. The fourth switch in IC13 is disabled, thereby releasing IC12-18 from 0V. When the listening device asserts that it is ready for data, the GPIA loads the contents of the data-out register onto the bus and continues with the handshake routine.

5.3.10.4.5 When the data-out register has been read, the GPIA generates a further interrupt request. The microprocessor resets IC17B, using line PB6, giving a logic 1 at IC18-12 so that the RFD line is again broken at IC13. The data transfer and data transmission sequence is then repeated.

5.3.10.5 Serial Poll

5.3.10.5.1 The status byte register of the GPIA is normally updated approximately every 1 ms by the microprocessor. When the interface is addressed to talk following the receipt of the serial poll enable (SPE) message, the GPIA puts the status byte onto the bus without further action by the microprocessor.

5.3.10.5.2 When the serial poll is completed, the controller sends the serial poll disable (SPD) message, which is detected by IC26, IC7, IC18, and IC19. The resulting logic 1 at IC17B-3 clocks IC17B to the reset condition, and gives a logic 1 at IC18-12.

5.3.10.6 Data Transfer Between Microprocessors

5.3.10.6.1 Data transfer between microprocessors is made using the multiplexed data bus on both devices. Connections between the buses is made by means of a D-type latch, IC1 or IC2, depending on the direction of data transfer. All data transfers are initiated by the sending device. The first byte indicates the number of bytes to be transferred.

5.3.10.6.2 For data transfer to the GPIB microprocessor, the instrument's microprocessor sets SK1 pin 22 ($\overline{\text{GPIBIRQ}}$) low. This provides an interrupt request (IRQ) to the GPIB microprocessor via IC4. As part of the interrupt routine, IC8 is enabled and addressed to give an enabling signal for IC5A. The microprocessor reads the IRQ flag via IC5A and data bus line 7 to establish that the IRQ is from the instrument and not the GPIA.

5.3.10.6.3 The GPIB microprocessor prepares to receive data, and then enables and addresses IC8 to give a signal which clocks IC16B via IC20-6. The level set on line 0 of the data bus is transferred to IC16B-5, and forms the ready for data (RFD) signal to the instrument's microprocessor.

5.3.10.6.4 The instrument's microprocessor enables and addresses IC3 to give an enabling signal to IC5B, reads the RFD signal, puts the first data byte on the bus, and readdresses IC3 to give a clock signal which latches the data into IC1. It then addresses IC3 to give a clock signal for IC16A, so that the logic level set at IC16A-12 is transferred to IC16A-19 to form the data valid (DAV) signal to the GPIB microprocessor.

5.3.10.6.5 The GPIB microprocessor addresses IC8 to give a signal to enable IC5A, and reads the DAV signal via data bus line 6. It then cancels its RFD signal, addresses IC8 to give an output enable signal for IC1 (via IC20-8) and reads the data. A data accepted (DAC) signal is sent via IC2 and the RFD signal is reset. The instrument's microprocessor responds by cancelling its DAV signal and entering the next data byte into IC1. Data transfer continues in this manner until the required number of bytes have been received.

5.3.10.6.6 Data transfer from the GPIB microprocessor to the instrument's microprocessor follows a similar pattern. The IRQ signal is passed from port A line 0 via IC18 and IC4. The IRQ flag is read by the instrument's microprocessor during its interrupt routine, via IC5B (enabled by an output from IC3). The IRQ signal is cancelled by the instrument's microprocessor setting data bus line 0 to logic 0 and then addressing IC3 to clock IC17A. The resulting logic 0 at IC17B-9 disables IC18-4.

5.3.10.6.7 During data transfer from the GPIB interface to the instrument, the RFD signal is passed via IC16A and IC5A, the DAV signal via IC16B and IC5B, the DAC signal via IC1, and the data via IC2.

6.1 INTRODUCTION

6.1.1 This section is written in eight parts including the following:

a. PVP/Calibration Inspection Intervals

b. Required Test Equipment

c. Dismantling and Reassembly

d. Special Functions for diagnostic purposes

e. Troubleshooting

f. Post-Repair Setup (or after the instrument fails the overall performance verification procedure)

g. Internal Frequency Standard - routine calibration

h. Overall Performance Verification Procedure

6.1.2 The Performance Verification Procedures (PVPs) provided in this section are used for (1) receiving inspection/acceptance, (2) periodic determination of the need for recalibration, (3) upon failure of a routine specification check, and (4) after repair of unit. Verify the basic operation of the counter before starting these procedures by completing the rapid functional check found in Subsection 2.6.

6.1.3 Satisfactory completion of these performance tests will confirm the counter's operation by measurement function. Complete the performance tests in the order given.

6.1.4 The following conditions must be maintained during these tests:

a. The counter must be operated from an AC supply

b. The line voltage must be within ±10% of the indicated value of the line voltage selector

c. The ambient temperature must be 23°C ±2°C except at receiving inspection/acceptance when a requirement of 23°C ±5°C is acceptable

d. The power supply to the internal frequency standard must remain uninterrupted. (This does not apply if the counter is locked to an external frequency standard.)

6.1.5 Warm up the counter for one hour (switched to standby if necessary) before beginning these procedures.

6.2 PVP/CALIBRATION INSPECTION INTERVALS

6.2.1 PVP Interval

6.2.1.1 First, refer to Subsection 6.1.2 and review those situations when PVPs should be performed. Periodic PVPs should be carried out, however, at least once a year to verify the basic operation of the 1992-02M and the possible need for recalibration.

6.2.2 Calibration Interval

6.2.2.1 The need for calibration is determined by the results of carrying out the set of PVPs, except in the case of the internal frequency standard. The calibration interval for the internal frequency standard will depend on the accuracy required and the aging rate of the 04E frequency standard installed. Simply divide the desired accuracy by the aging rate per day to determine the required calibration interval for the internal standard.

NOTE:

All other calibration points for the 1992-02M except the internal frequency standard should be on a minimum annual basis.

6.3 REQUIRED TEST EQUIPMENT

6.3.1 A complete list of the test equipment required to carry out the procedures described in this section is given in Table 6.1. The items required for each operation are listed at the start of the corresponding instructions.

6.3.2 A particular model of test equipment is recommended in some cases, but other equipment having the required parameters given in Table 6.1 may be used. Although the procedures to be followed are given in general terms, they are based on the use of the recommended test equipment. Some modification to the procedure may be necessary if other test equipment is used.

6.4 DISMANTLING AND REASSEMBLY

6.4.1 Introduction

6.4.1.1 Instructions for dismantling and reassembling the instrument are limited to those areas where special care is needed or difficulty may be experienced.

WARNING

LETHAL VOLTAGE: Dangerous AC voltages are exposed when the instrument is connected to the AC supply with the covers removed. Switch the instrument off and disconnect the supply socket from the rear panel before carrying out any dismantling or reassembly operation.

Table 6.1 - Required Test Equipment

Item	Description/Recommended Model	Required Parameters
1	Signal Generator Racal-Dana 9087	Low phase noise. Jitter < 0.5 ns. Frequency range 10 kHz to 1.3 GHz. Output level 1 mV to 1V 10 MHz INT STD OUTPUT
2	Oscilloscope with 1:1 Probe	Bandwidth 50 MHz
3	Digital Multimeter Racal-Dana 5001	Frequency range: DC to 5 kHz Level: 20 mV to 20V
4	Frequency Standard Racal-Dana 9475	10 MHz Accuracy better than ±3 parts in 10^{10}
5	Audio Oscillator Racal-Dana 9085	Frequency range: 10 Hz to 5 kHz Level: 30 mV into 50Ω
6	Pulse Generator Racal-Dana 1515	To provide a single positive-going pulse with a low level of +0.4V and a high level of +2.4V (TTL output limit levels)
7	Connecting Lead	50Ω coaxial cable with BNC connectors. Length between 60 cm and 1m
8	T-piece	BNC, 50Ω
9	Coaxial Load	BNC, 50Ω
10	GPIB Controller HP-85	—
11	GPIB Analyzer Racal-Dana 488	—

6.4.2 Instrument Covers

6.4.2.1 Complete the following procedure to remove the instrument covers:

a. Disconnect the power cord from the rear panel

b. Remove the two screws and washers securing the rear-panel bezel shown in Figure 6.1. Then remove the bezel

c. Remove the top cover by sliding it to the rear of the instrument

d. Remove the bottom cover by sliding it to the rear of the instrument

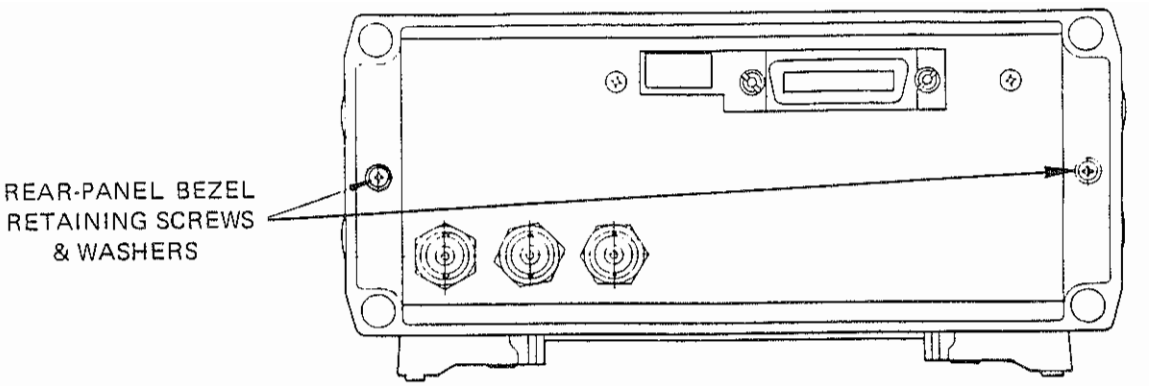


Figure 6.1 - Rear-Panel Bezel Removal

6.4.2.2 To replace the covers, reverse the above procedure. When replacing the bottom cover, ensure that the tilt bail is facing toward the front of the instrument and that the tongue of the cover fits into the slot on the front panel as shown in Figure 6.2. When replacing the top cover, ensure that the access holes are towards the front of the instrument (see Figure 6.3) and that the tongue of the cover fits under the edge of the front panel at all points. Refer to Figure 6.4 for orientation of the bezel to the rear panel.

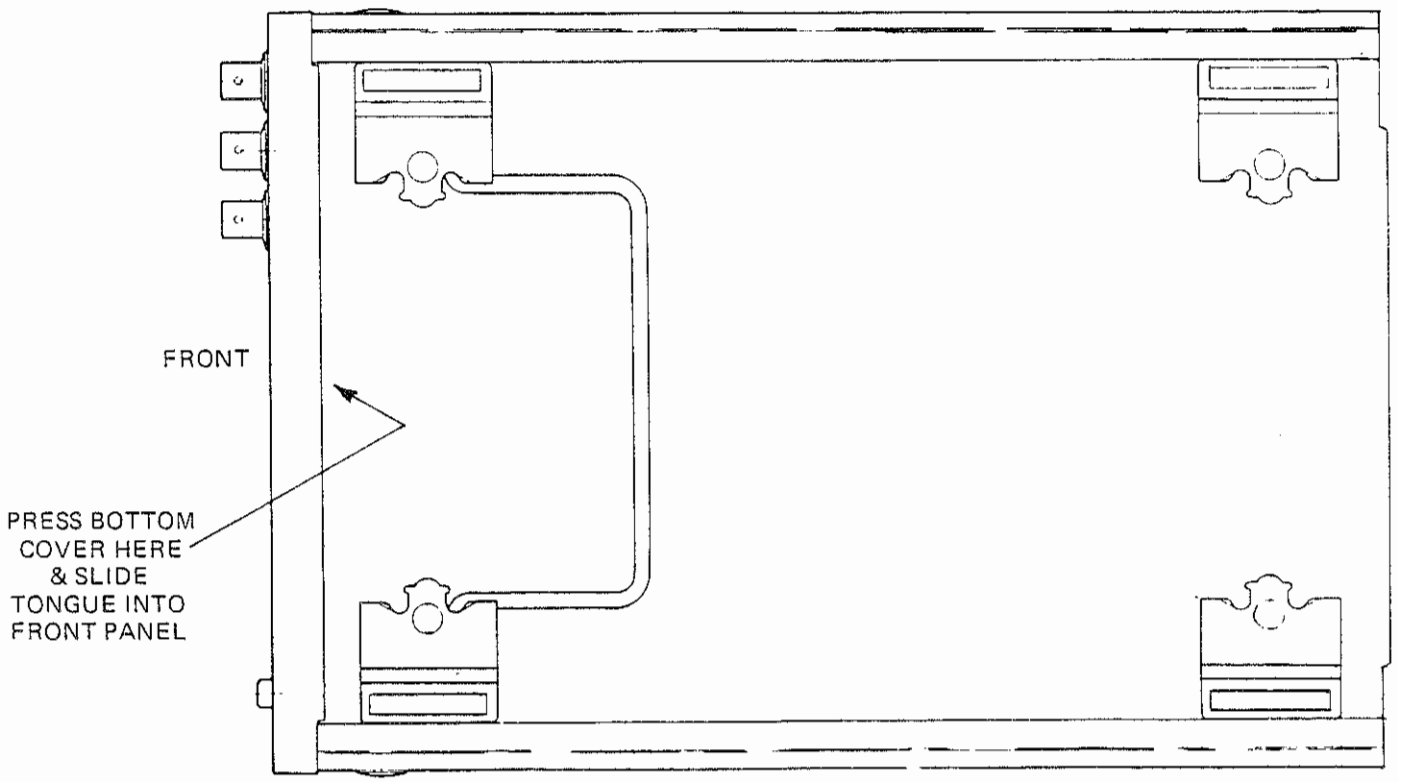


Figure 6.2 - Bottom Cover Replacement

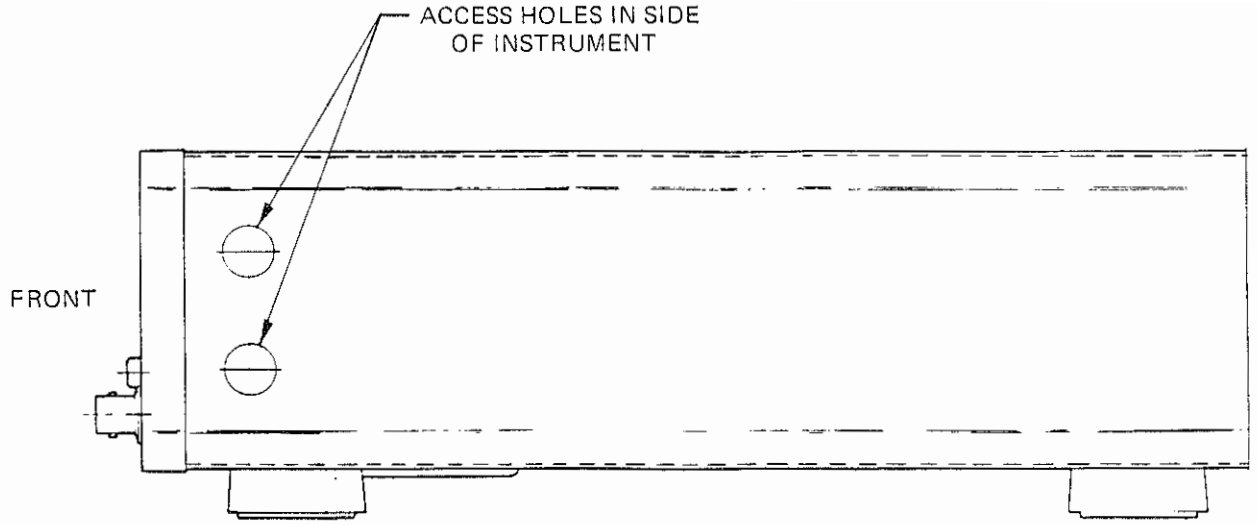


Figure 6.3 - Proper Access Hole Orientation

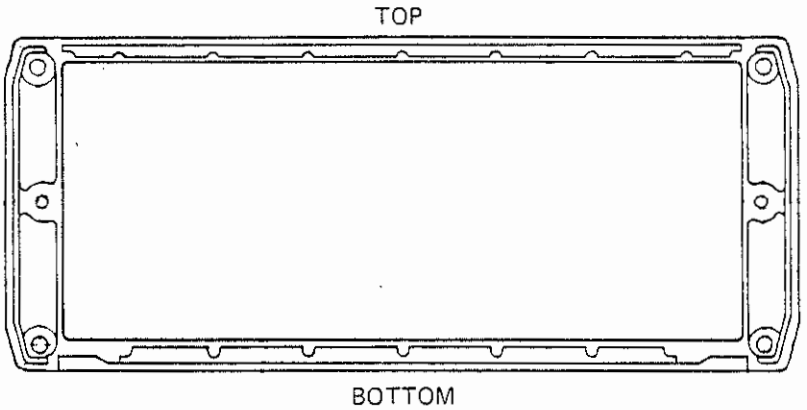


Figure 6.4 - Rear Panel Bezel Orientation

6.4.3 Front Panel

6.4.3.1 Complete the following procedure to remove the instrument front panel:

a. Remove the top and bottom covers of the instrument

b. Remove the clamping collars from the channel A and B inputs. Use the special spanner available from Racal-Dana (P/N R-14-1586) and turn counterclockwise. Refer to Figures 6.5A and 6.5B for this step

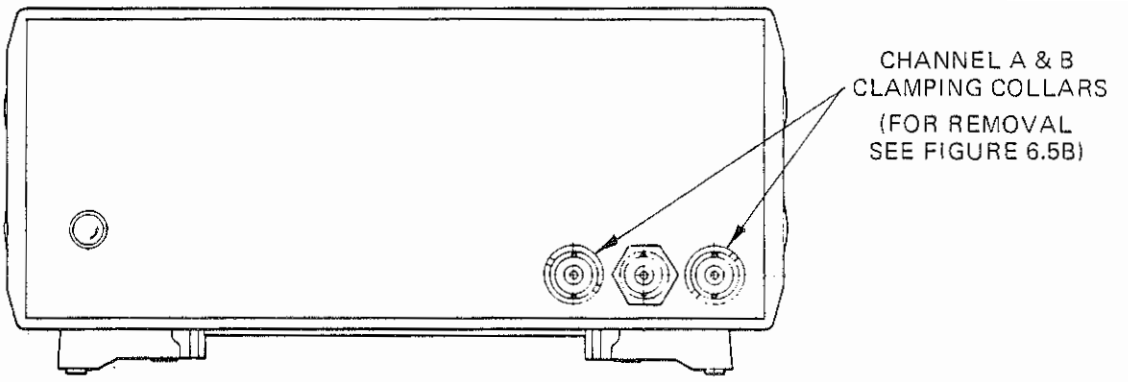


Figure 6.5A - Channel A and B Clamping Collars

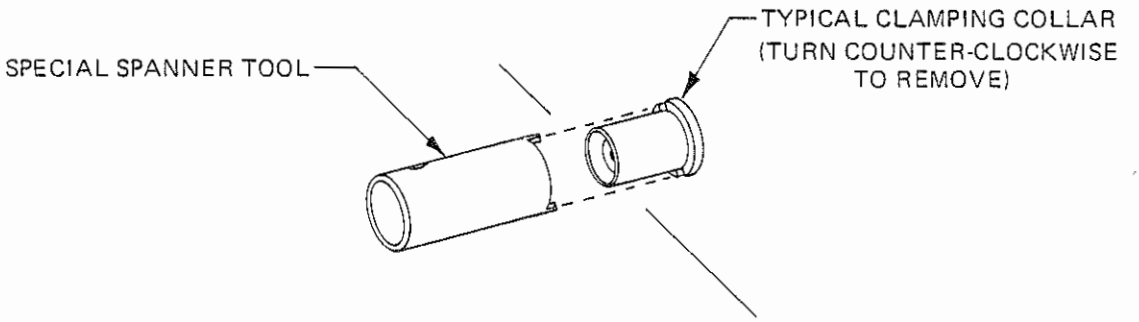


Figure 6.5B - Clamping Collar Removal

c. Remove the two screws and washers securing the front panel to each side frame of the instrument. See Figure 6.6

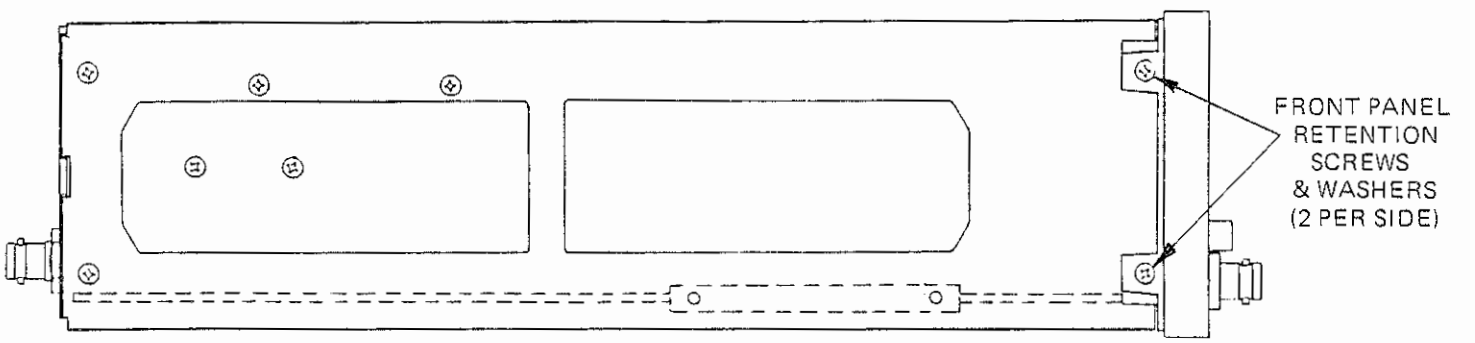


Figure 6.6 - Front-Panel Retention Screw Removal

d. Ease the front panel forward until the display board disconnects from the motherboard at PL1 and PL2. See Figure 6.7

e. Disconnect the coaxial lead from the back of the Channel C input. See Figure 6.7

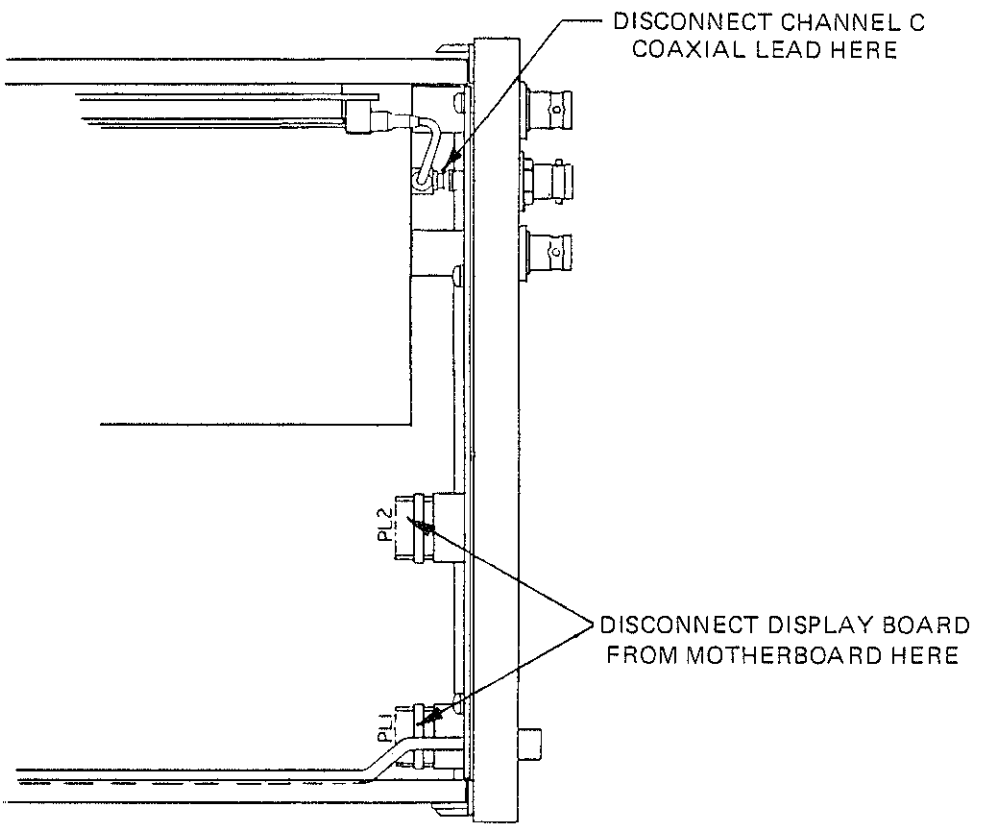


Figure 6.7 - Display Board and Channel C Disconnection

6.4.3.2 To replace the front panel, reverse the above procedure. Pass the POWER switch button through its opening in the front panel and reconnect Channel C's coaxial lead to the PCB to Channel C's input connector before securing the panel.

6.4.4 Rear Panel

6.4.4.1 Complete the following procedure to remove the instrument rear panel:

a. Remove the instrument covers

b. Refer to Figure 6.8. Remove the GPIB board from the unit by completing the following steps:

1. Remove the two screws and lock washers on the rear panel as shown

2. Remove the two screws on the GPIB board itself as shown

3. Lift up the GPIB board where shown and unplug the GPIB/motherboard cable from the motherboard at SK4

4. Now the GPIB board is free to remove

c. Remove the two screws and washers (2 each/side) securing the rear panel to each side frame of the instrument. See Figure 6.9

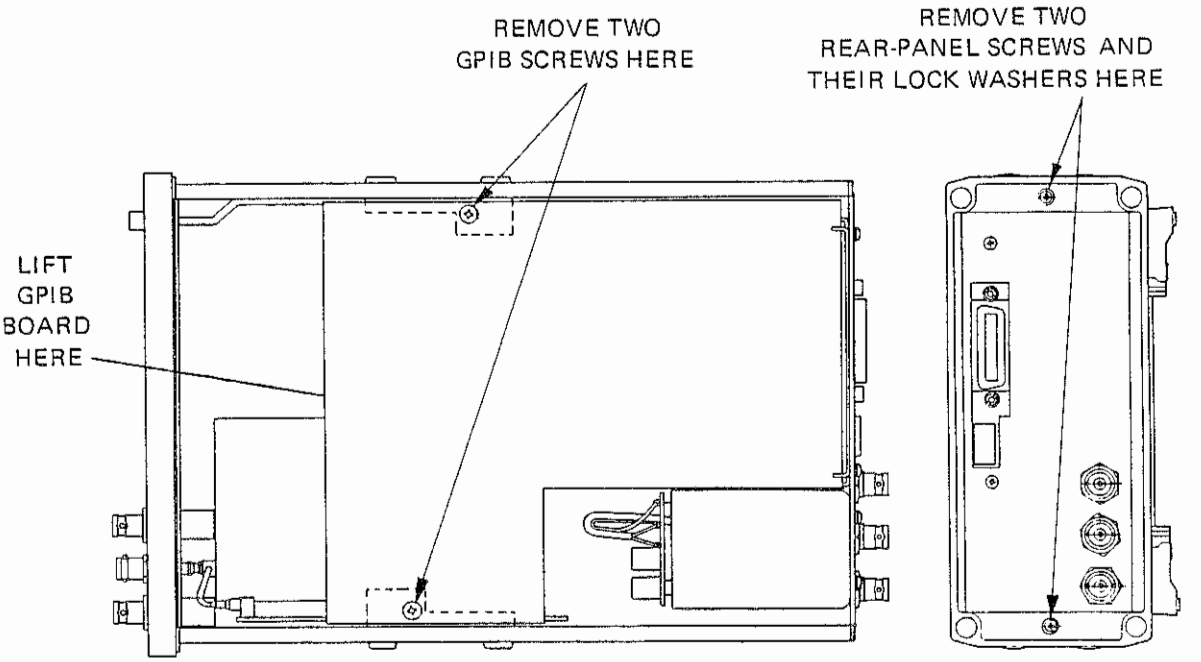


Figure 6.8 - GPIB Board Removal

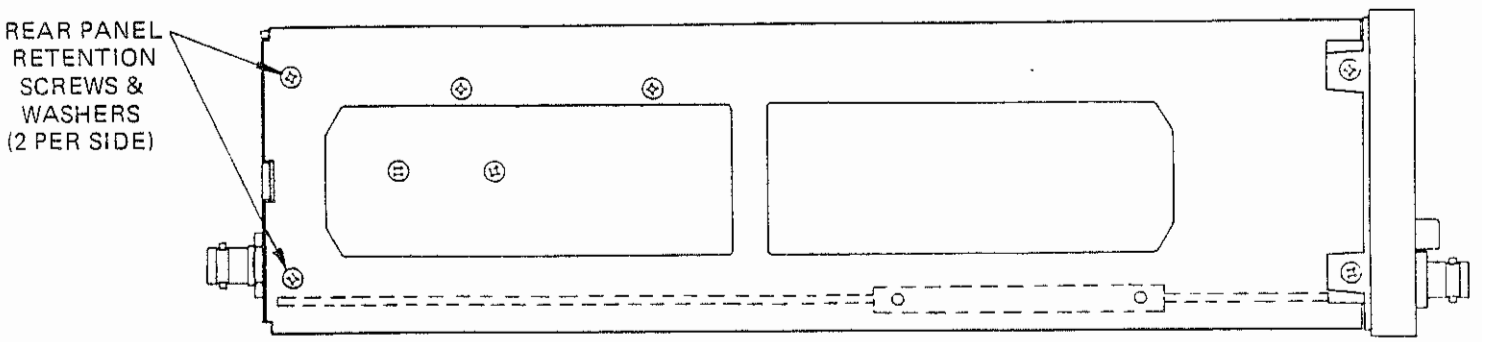


Figure 6.9 - Rear-Panel Retention Screw Removal

d. Ease the rear panel away from the instrument and disconnect from the motherboard at PL19 and PL20. See Figure 6.10

e. Disconnect the frequency standard's flying lead from PL14 on the motherboard. See Figure 6.10

f. Remove the nut and crinkle washer securing the rectifier bridge D11 to the rear panel. See Figure 6.10

g. Disconnect the green/yellow lead connecting the rear-panel stud to the power input plug. See Figure 6.10

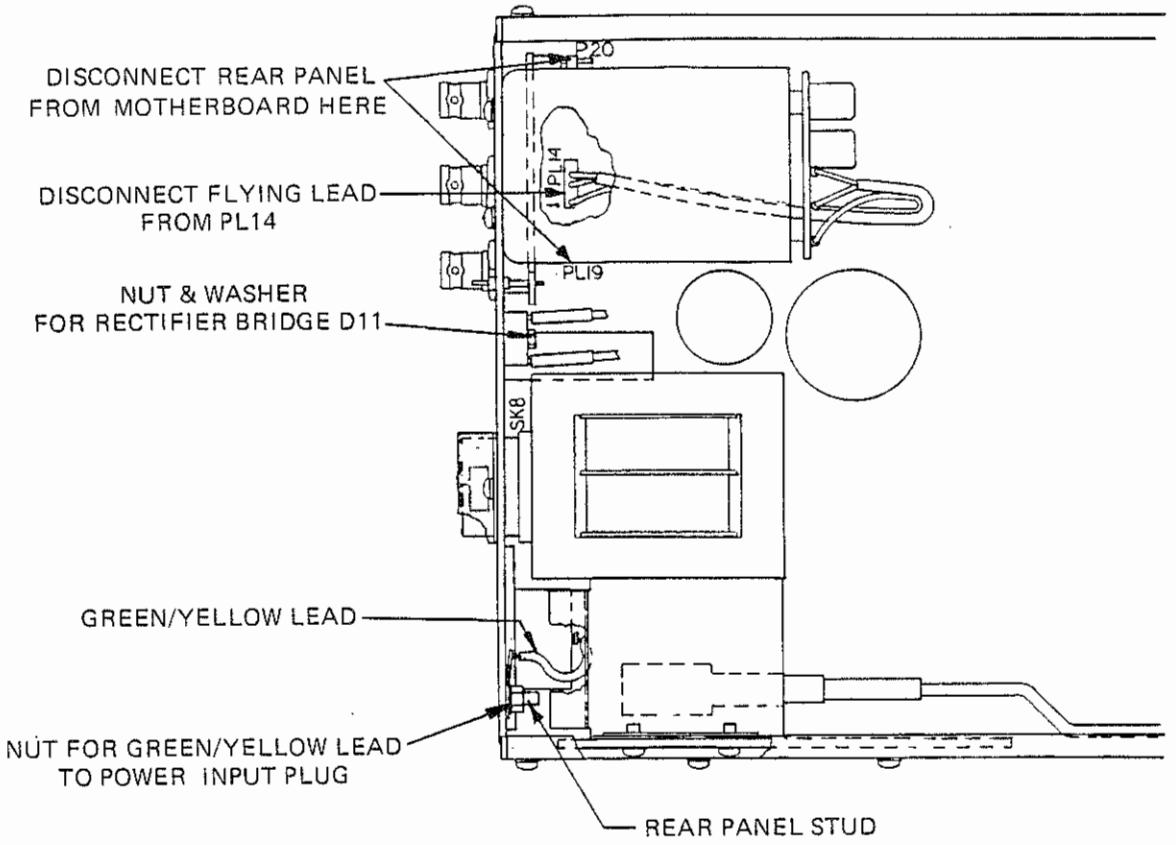


Figure 6.10 - Rear-Panel Removal Detail

6.4.4.2 To replace the rear panel, reverse the above procedure.

WARNING

LETHAL VOLTAGE - the grounding of external metalwork of the instrument depends upon the connection between the rear-panel stud and the power input plug. Ensure that the green/yellow lead to the power input plug is correctly connected during reassembly.

6.4.5 Channel C Board

6.4.5.1 Complete the following procedure to simply access Channel C's PCB:

a. Remove the top cover

b. Remove GPIB board. Refer to Subsection 6.4.4.1.b for instructions

c. Remove the two screws and washers securing Channel C's amplifier PCB to the right-hand side frame. See Figure 6.11

6.4.5.2 Complete the following steps to remove the amplifier board completely:

a. Remove the front panel (see Subsection 6.4.3)

b. Disconnect the coaxial lead from the back of Channel C's input

6.4.5.3 To replace the amplifier board, reverse the above procedure.

6.4.6 Display Board

6.4.6.1 Complete the following procedure to remove the display board:

a. Remove the instrument covers (see Subsection 6.4.2)

b. Remove the front panel (see Subsection 6.4.3)

c. Remove the three screws and washers securing the display board to the front panel (see Figure 6.11) and remove the board

6.4.6.2 To replace the display board, reverse the above procedure.

6.5 SPECIAL FUNCTIONS FOR DIAGNOSTIC PURPOSES

6.5.1 The special functions listed in Table 6.2 are for use during maintenance. The functions are used in conjunction with the CHECK mode. They are entered in the special function register by pressing:

[N] [N] [SHIFT] [STORE] [SF]

and are enabled and disabled by pressing

[SHIFT] [SF]

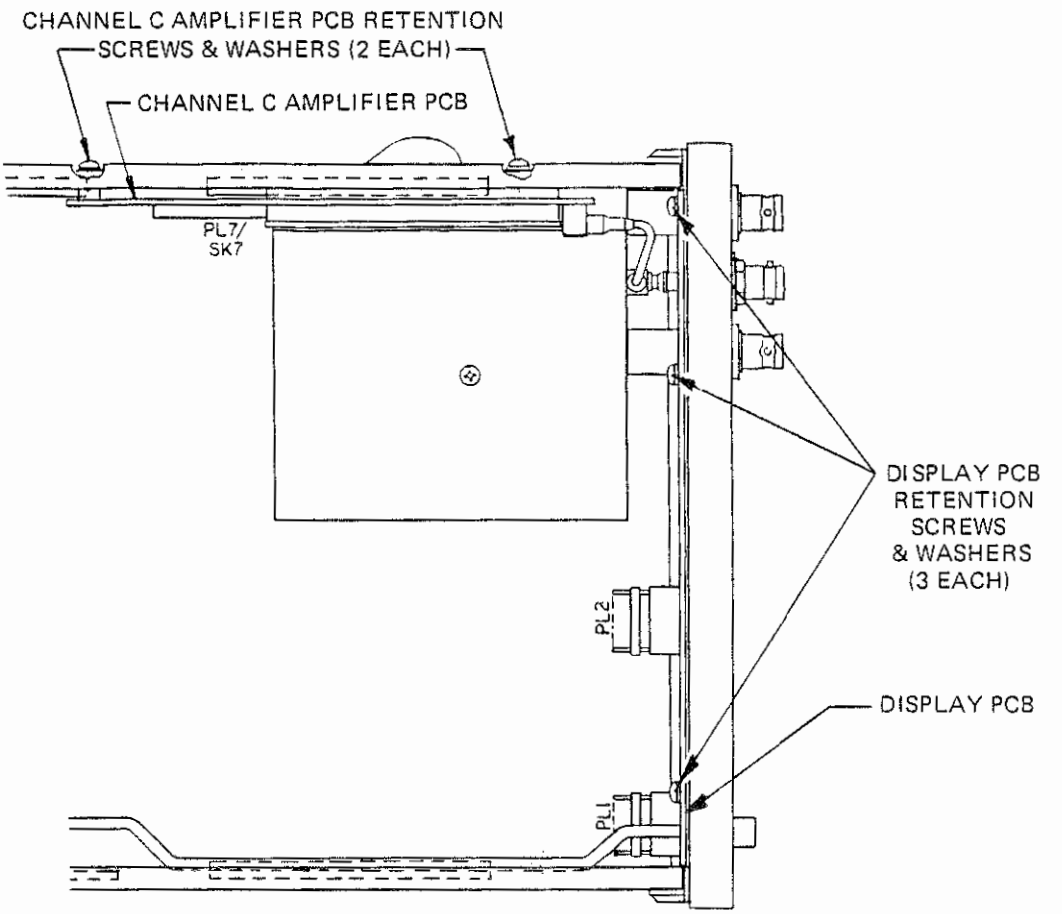


Figure 6.11 - Channel C Board and Display Board Removal

Table 6.2 - Diagnostic Special Functions

Special Function Number	Function With CHECK Mode Selected
70	10 MHz check
71	LED check
72	Measurement of short start TEC count
73	Measurement of long start TEC count
74	Measurement of short stop TEC count
75	Measurement of long stop TEC count
76	D-to-A converter check
77	Channel A relay check
78	Channel B relay check

6.5.2 Special Function 70

6.5.2.1 Special Function 70 is the default state of its decade. It provides measurement of the 10 MHz internal frequency standard and verifies operation of the microprocessor system, MCC1, MCC2, and the TEC.

6.5.3 Special Function 71

6.5.3.1 Special Function 71 exercises all the LEDs, except STANDBY, GATE, TRIG A, TRIG B, REM, ADDR and SRQ, at approximately 0.5 Hz. If the GPIB interface is fitted, the REM, ADDR and SRQ indicators light.

6.5.4 Special Functions 72, 73, 74, and 75

6.5.4.1 Special Functions 72, 73, 74, and 75 should only be used for diagnostic purposes at an ambient temperature of $23^{\circ}C \pm 2^{\circ}C$.

6.5.4.2 The long counts must be 800 ± 220. The short counts (0.5 x long count) must be in the range +20 to -40. Counts outside these ranges indicate that the TEC has failed.

6.5.5 Special Function 76

6.5.5.1 With Special Function 76 active, the microprocessor continuously exercises the D-to-A converters in both Channel A and Channel B through the range -5.1V to +5.1V. The waveform (51 levels spaced by 0.2V) can be monitored at the trigger output pins on the rear panel.

6.5.6 Special Function 77

6.5.6.1 With the 10 MHz STD OUTPUT socket on the rear panel connected to the Channel A input, activating Special Function 77 causes the microprocessor to exercise the Channel A relays for x10/x1, 50Ω/1 MΩ and DC/AC, FILTER, and COM A. See NOTE below.

6.5.7 Special Function 78

6.5.7.1 With the 10 MHz STD OUTPUT socket on the rear panel connected to the Channel B input, activating Special Function 78 causes the microprocessor to exercise the Channel B relays for x10/x1, 50Ω/1 MΩ and DC/AC. See NOTE below.

NOTE:

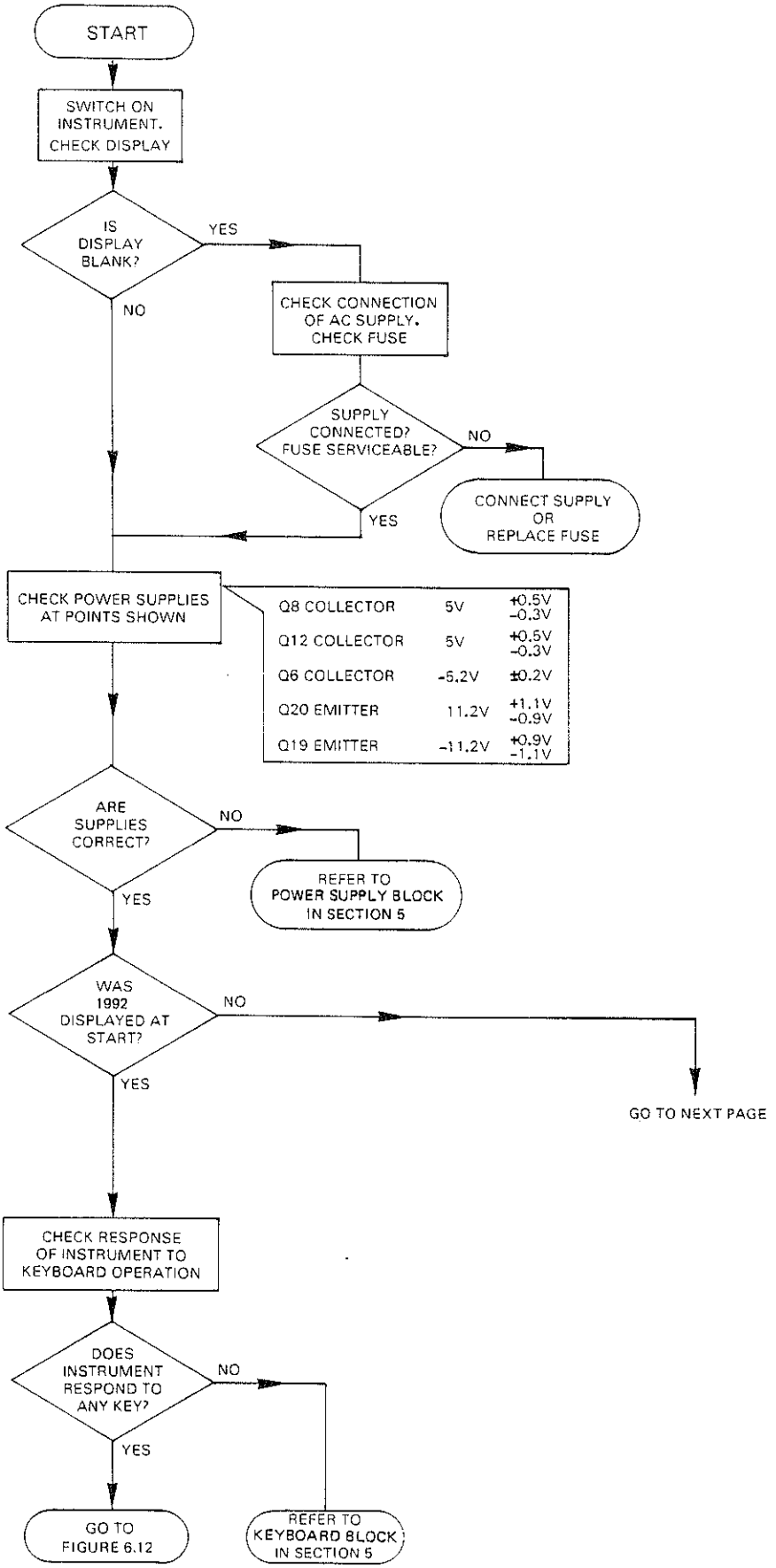
Cable length is important during use of either Special Function 77 or 78 for diagnostic purposes. The cable should be between 0.6 to 1 meter in length. See Item 7 in Table 6.1.

6.6 TROUBLESHOOTING

6.6.1 A guide to fault location is given in the flowcharts of Figures 6.12 to 6.19. The charts provide a logical procedure for localizing the fault to an area of circuit. When using the charts it is essential to begin at the start point in Figure 6.12 or 6.17 and act in sequence according to the results of each decision box. Starting part way through any chart is unlikely to lead to satisfactory fault isolation.

6.6.2 Required Test Equipment

Item	Table 6.1, Item No.
Oscilloscope	2
Digital Multimeter	3
Coaxial Connecting Lead	7
GPIB Controller	10
GPIB Analyzer	11



ure 6.12 - Fault Finding Flowchart - Part 1

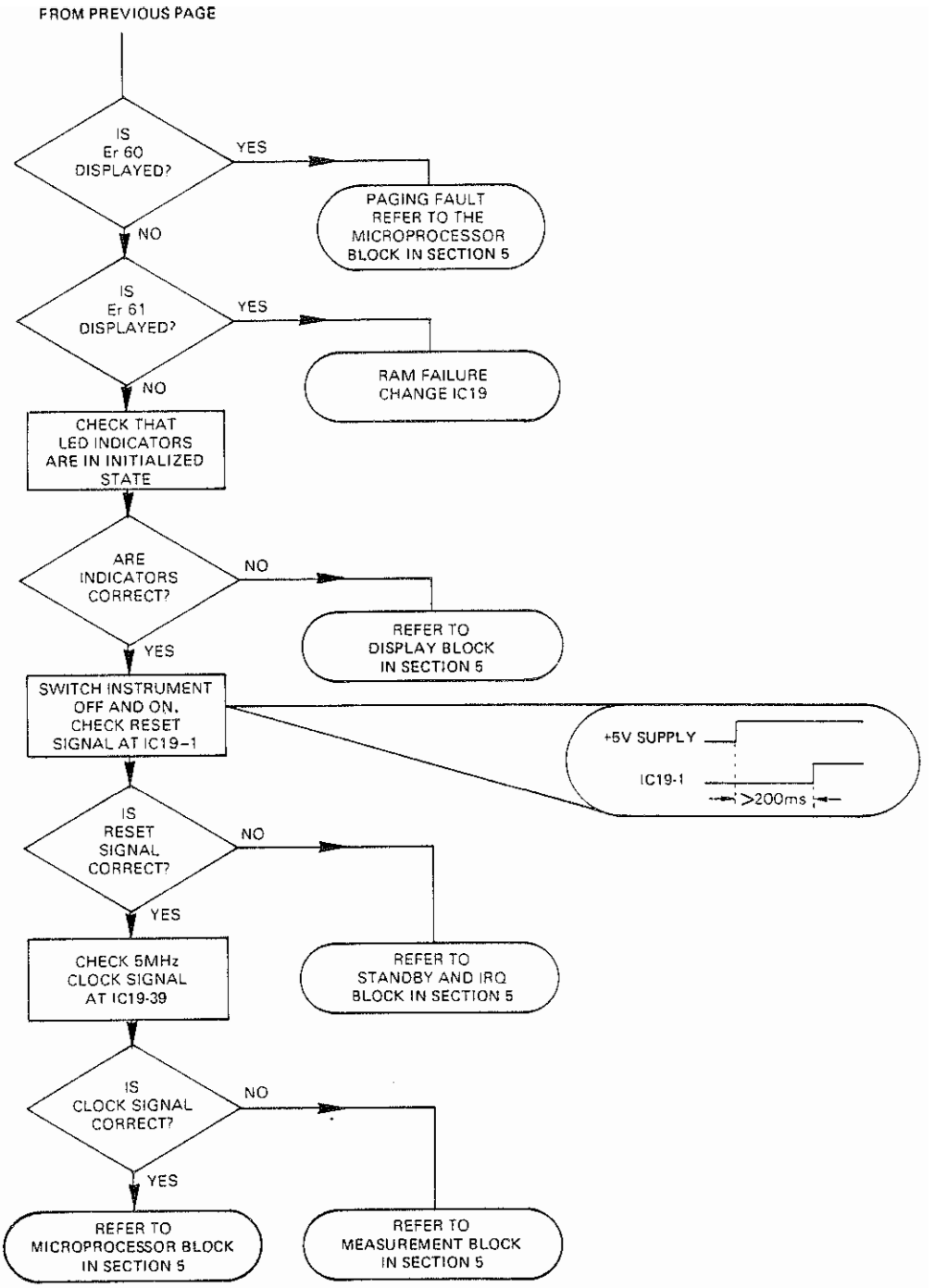


Figure 6.12 - Fault Finding Flowchart - Part 1 (Cont'd)

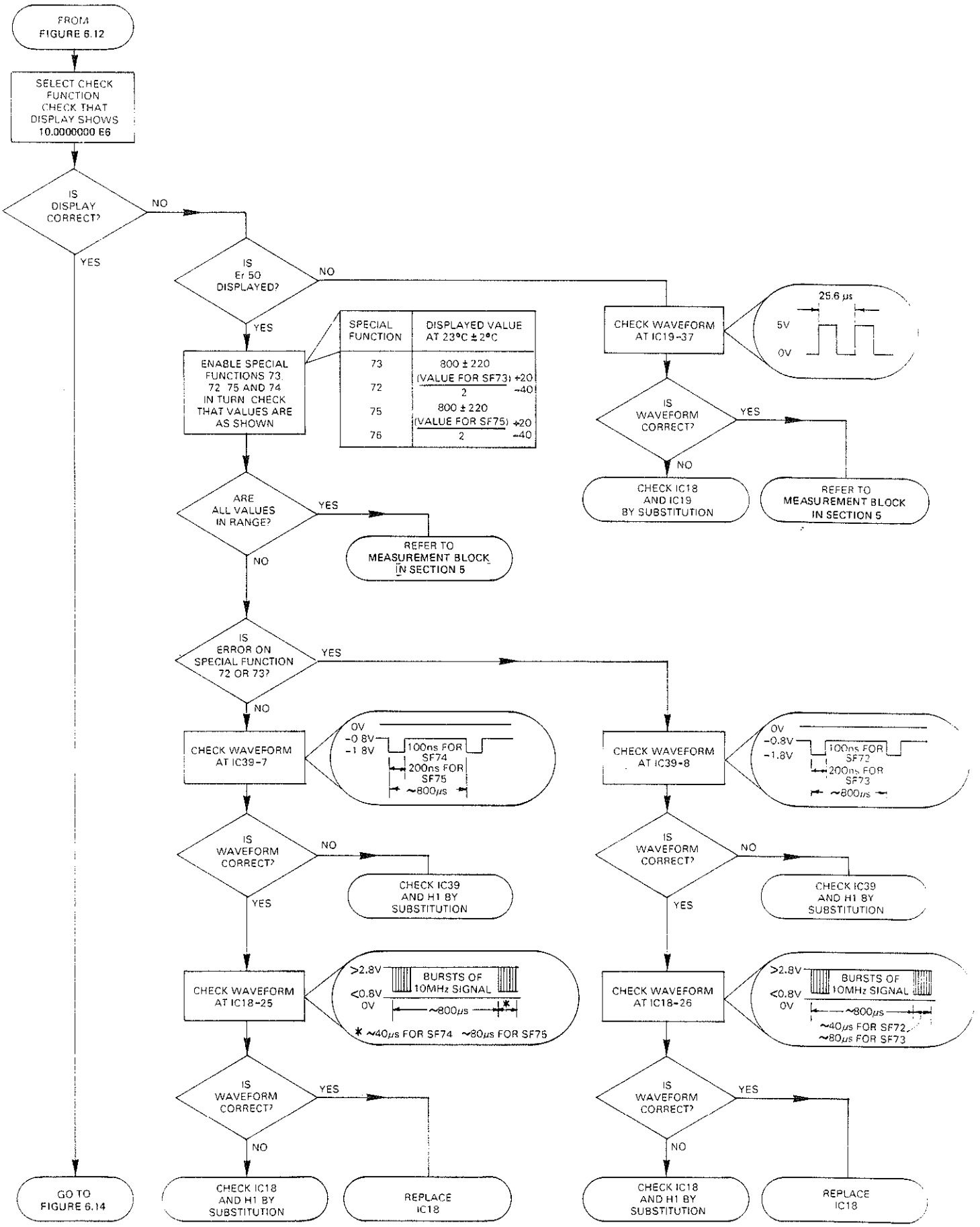


Figure 6.13 - Fault Finding Flowchart - Part 2

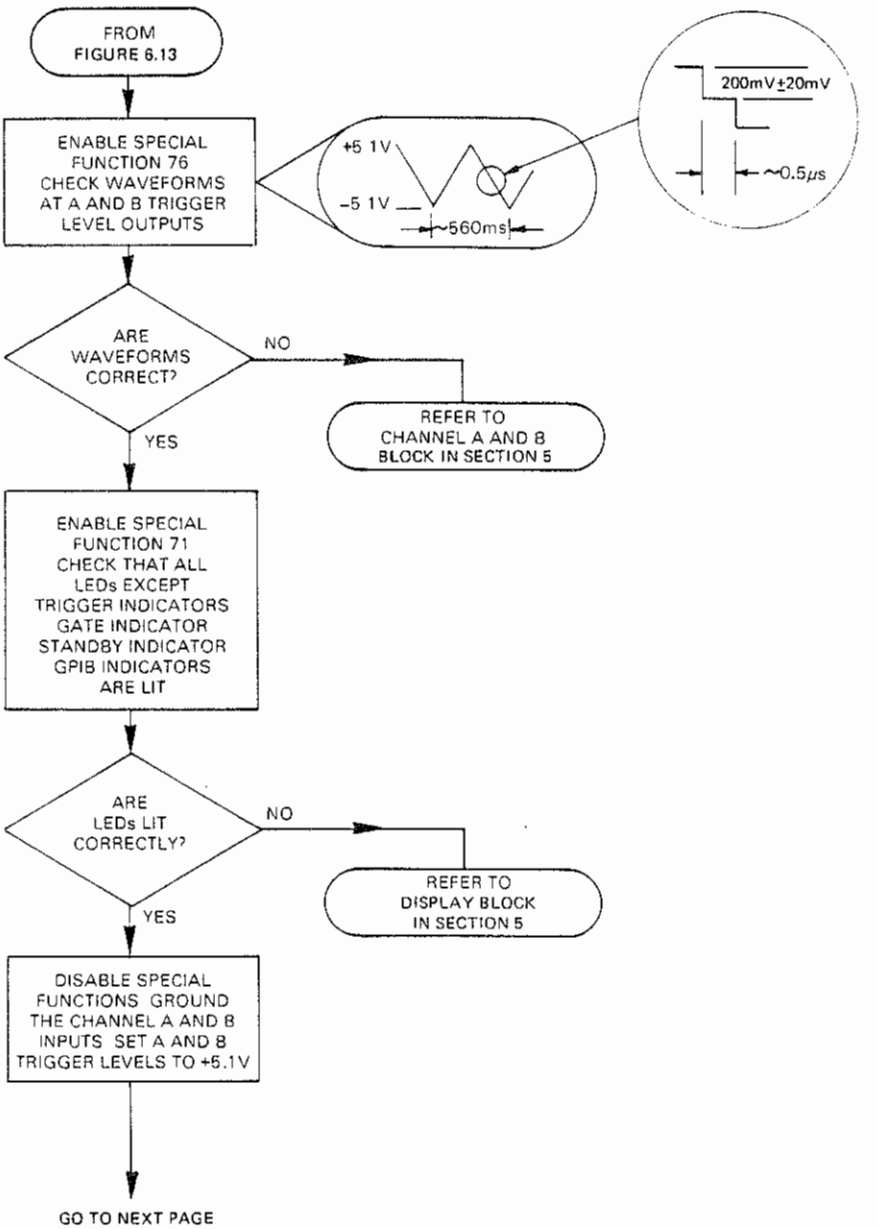
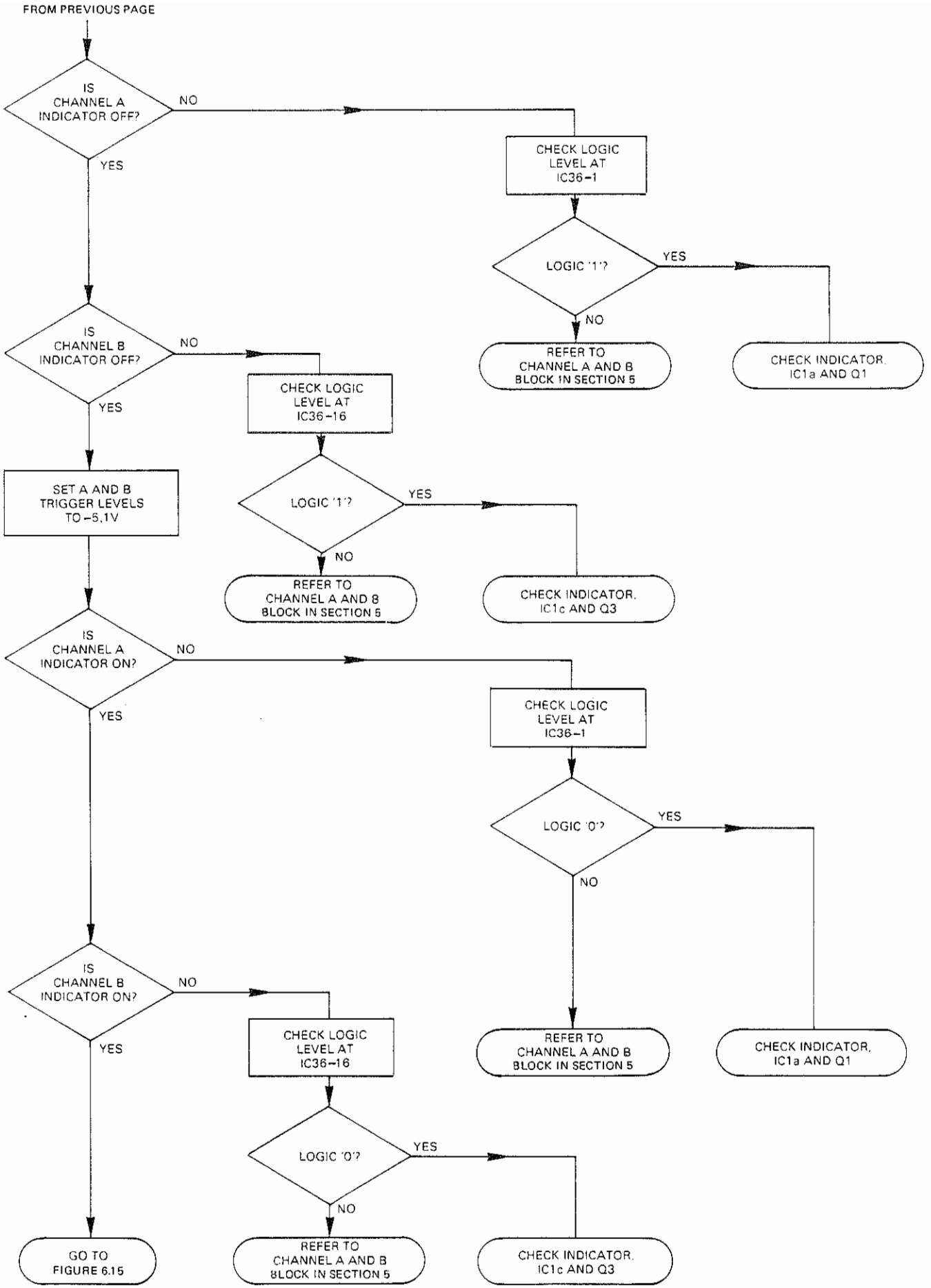


Figure 6.14 - Fault Finding Flowchart - Part 3



6.14 - Fault Finding Flowchart - Part 3 (Cont'd)

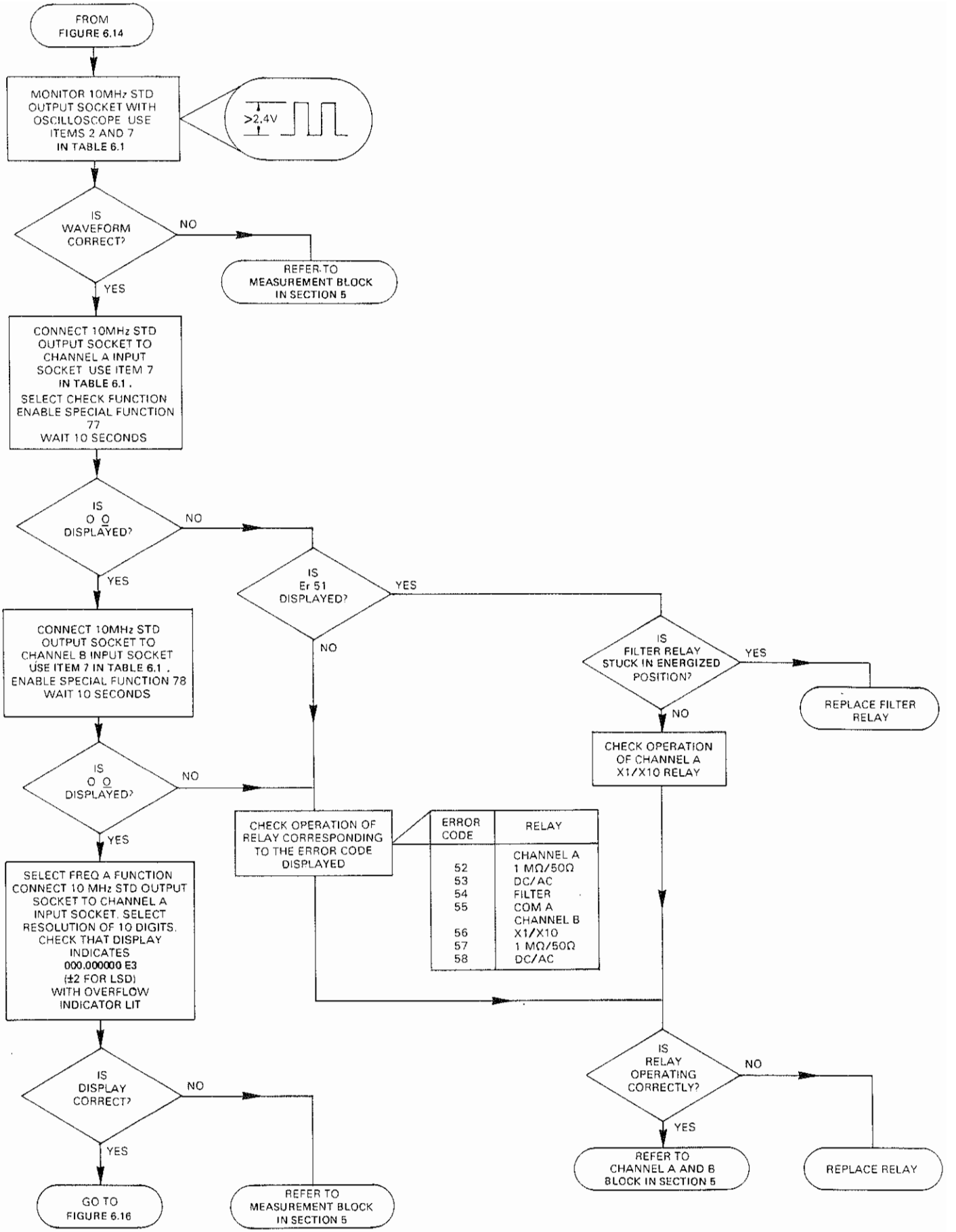


Figure 6.15 - Fault Finding Flowchart - Part 4

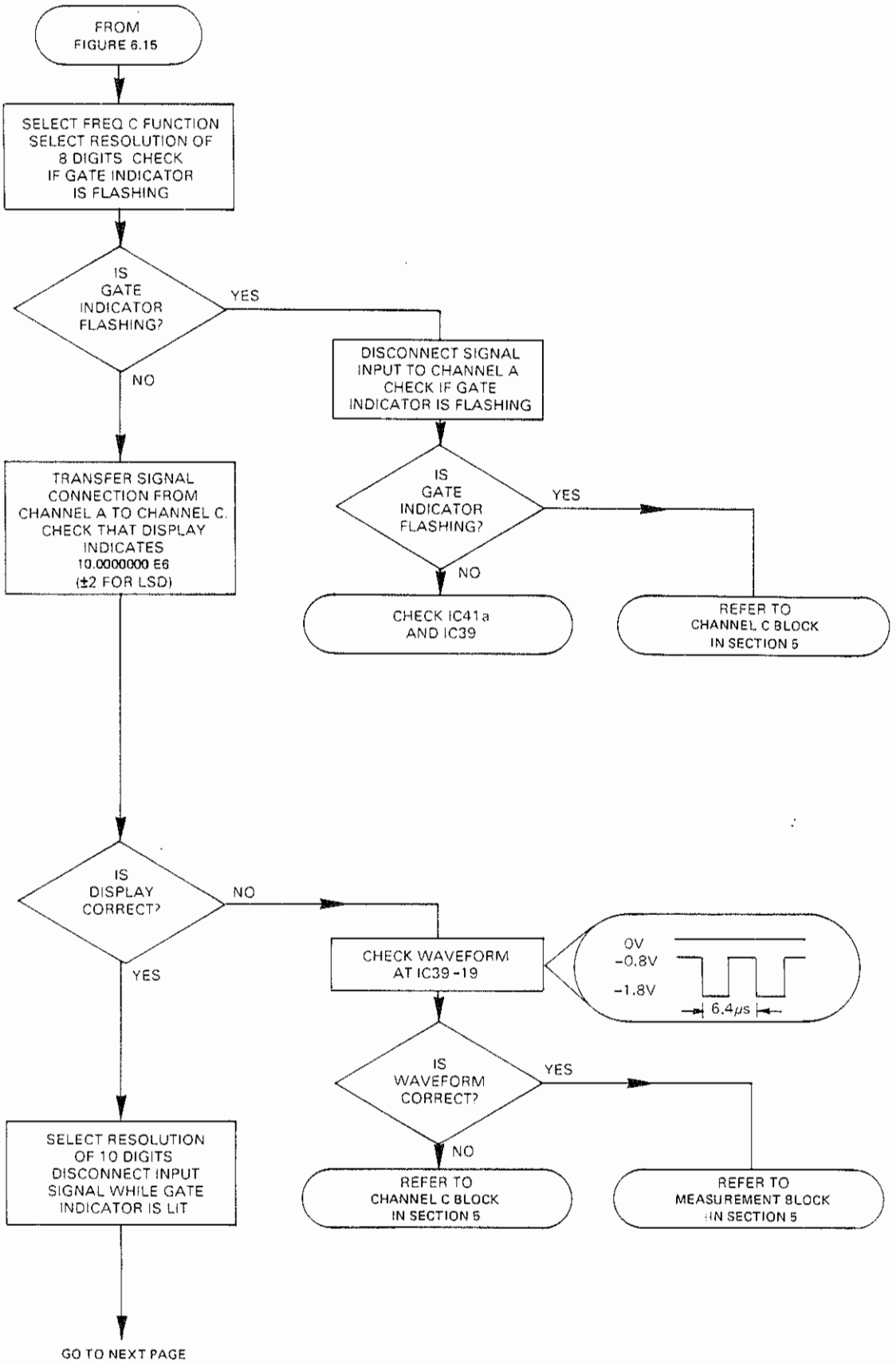


Figure 6.16 - Fault Finding Flowchart - Part 5

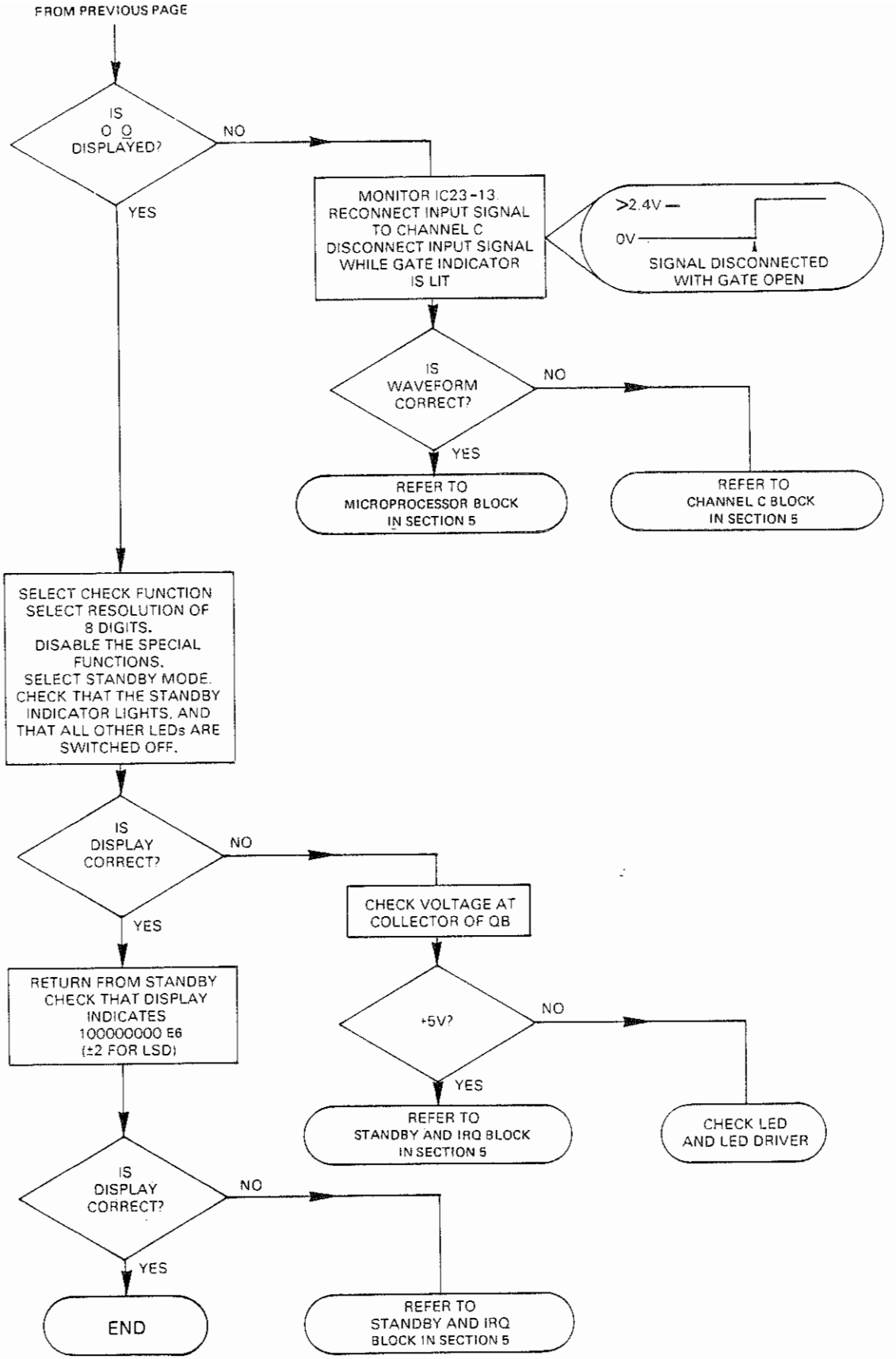


Figure 6.16 - Fault Finding Flowchart - Part 5 (Cont'd)

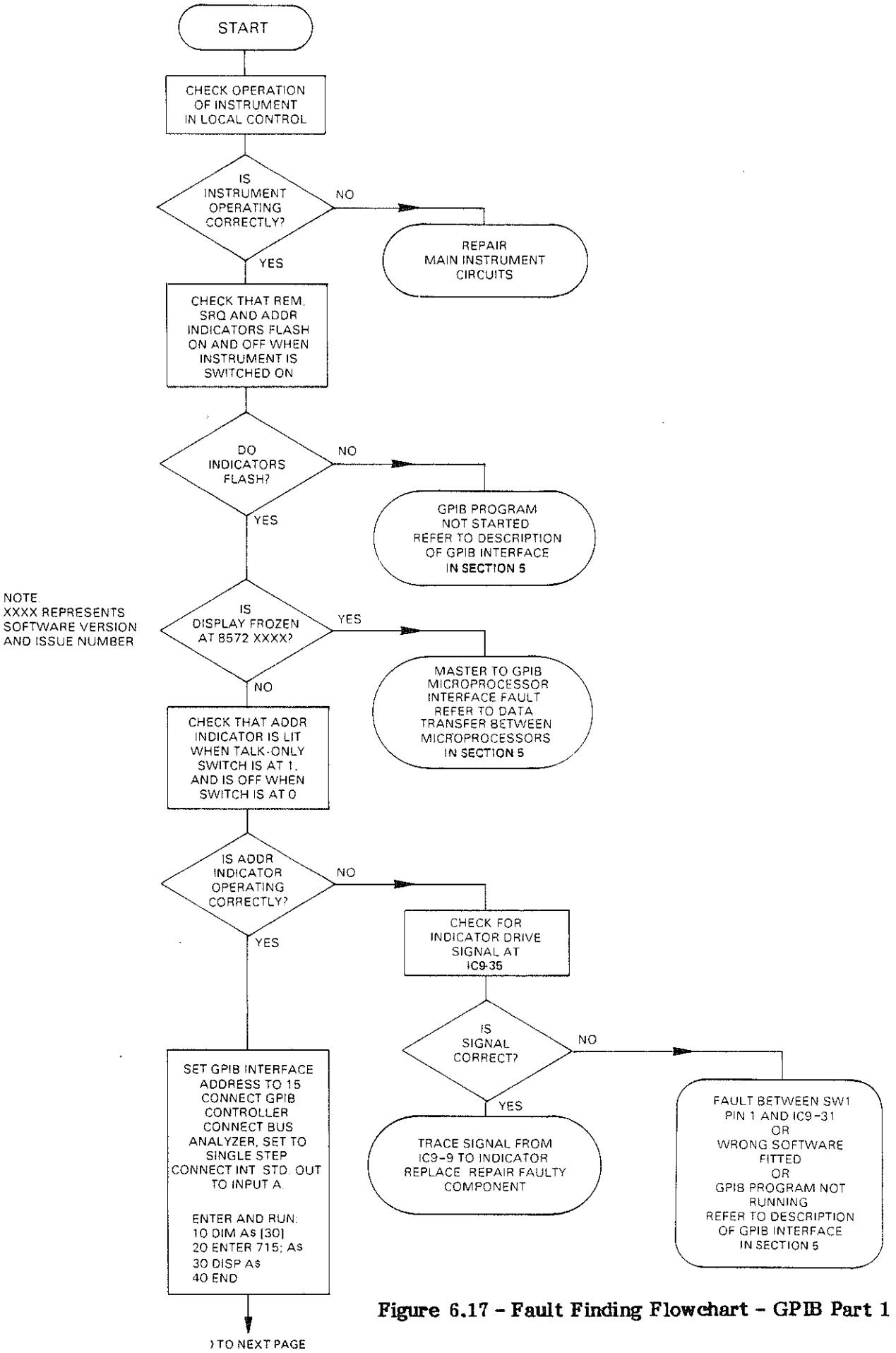


Figure 6.17 - Fault Finding Flowchart - GPIB Part 1

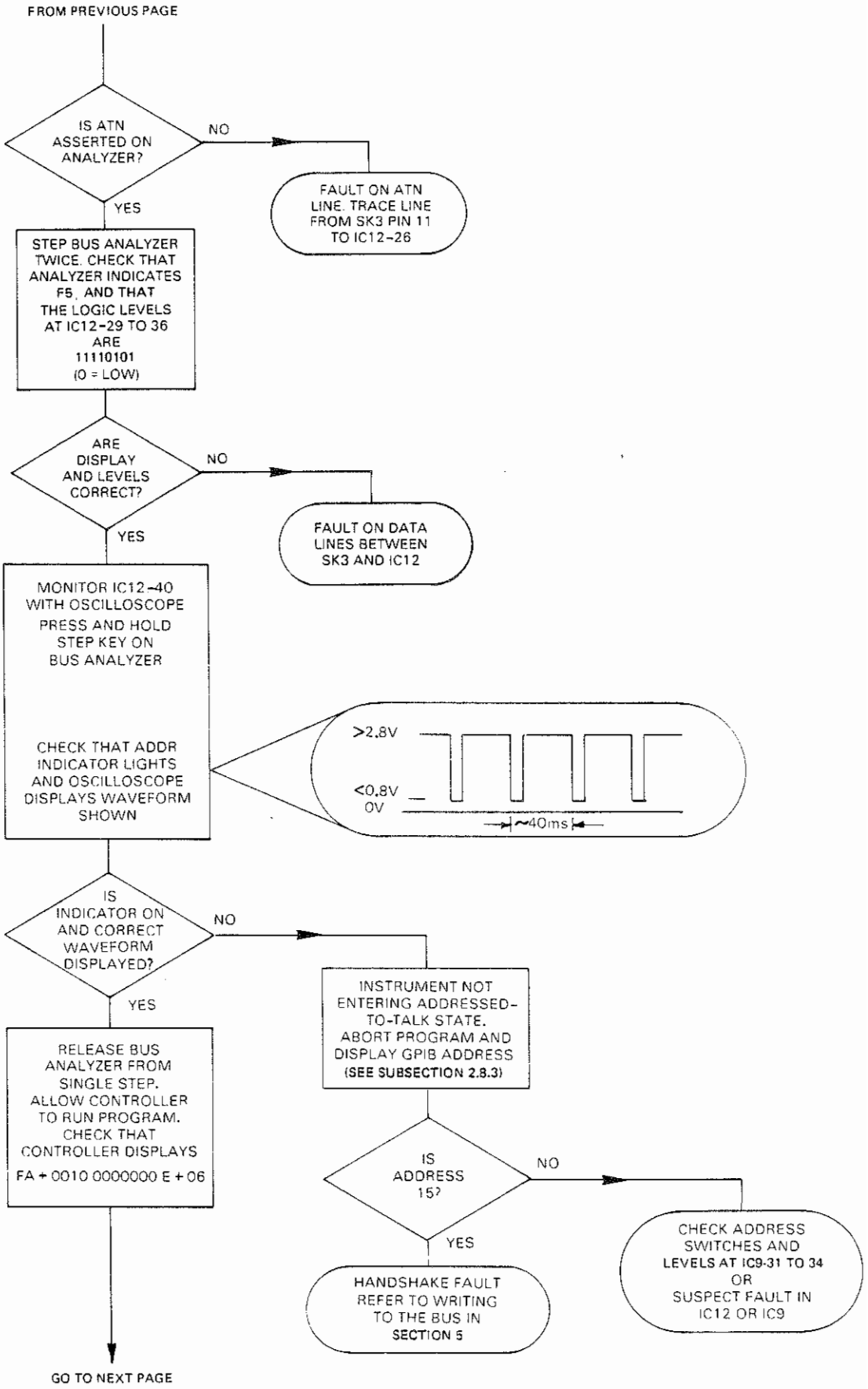


Figure 6.18 - Fault Finding Flowchart - GPIB Part 2

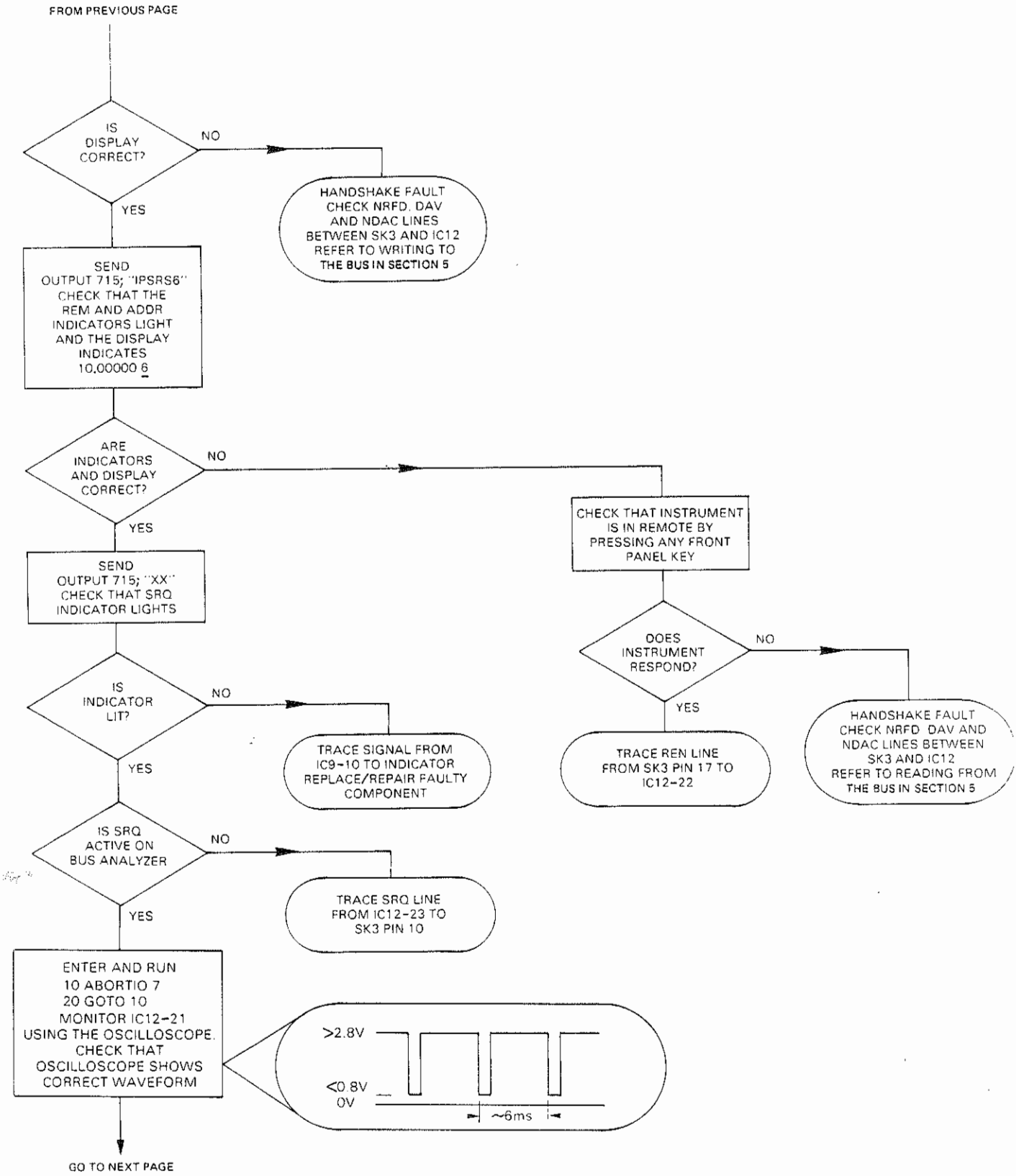


Figure 6.19 – Fault Finding Flowchart – GPIB Part 3

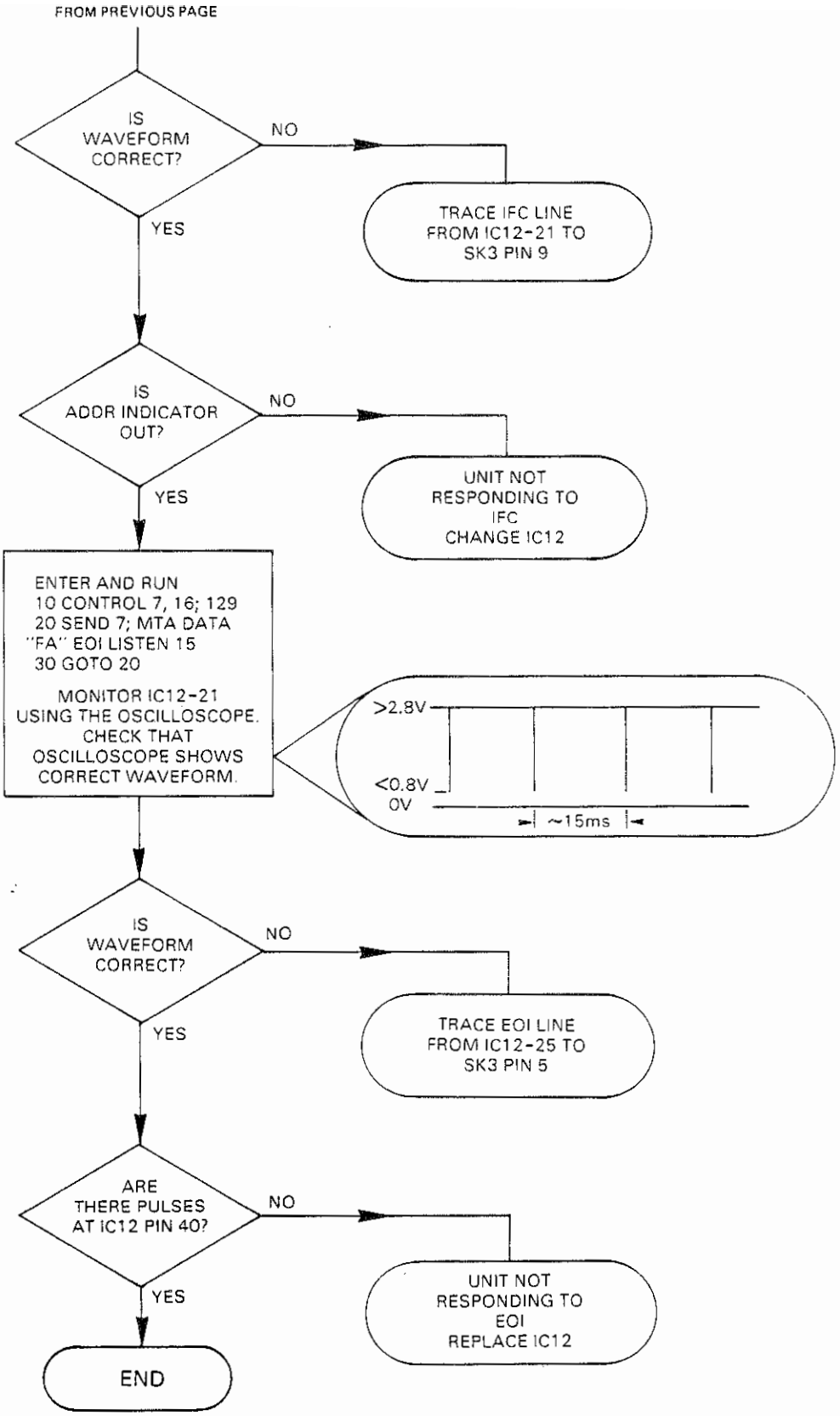


Figure 6.20 - Fault Finding Flowchart - GPIB Part 4

6.7 POST-REPAIR SETUP

6.7.1 Introduction

6.7.1.1 After repair, implement the appropriate setup procedure from the following subsections before performing the overall performance verification. These procedures should also be used if the instrument fails the overall performance verification check.

6.7.1.2 The ambient temperature must be maintained at 23°C ± 2°C throughout these procedures. The instrument should be powered from an AC supply.

WARNING

LETHAL VOLTAGE: These procedures require the instrument to be operated with the covers removed. Lethal voltage levels are exposed under these conditions.

6.7.2 Channel A Input System

6.7.2.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Coaxial Connecting Lead (Qty. 2)	7

6.7.2.2 Counter Setup Procedure

6.7.2.2.1 Set R149 fully counter-clockwise and R192 to its mid-position. R192 is located inside the screened module as shown in Figure 6.21.

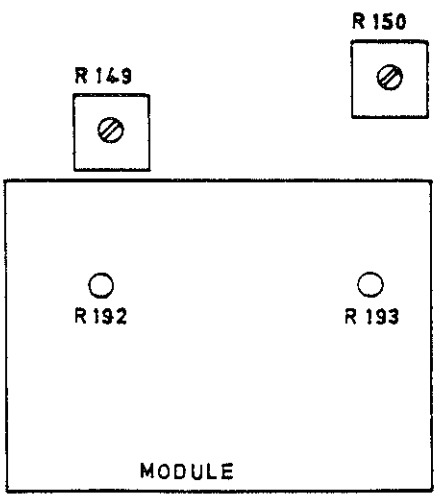


Figure 6.21 - Location of R149 and R192

6.7.2.2.2 Complete the following procedure:

a. Switch the 1992-02M on. Select FREQ A

b. Select 50Ωimpedance for Channel A

c. Press the RESOLUTION ↓ key five times until 000 is displayed

d. Connect the test equipment as shown in Figure 6.22

e. Set the signal generator output to 100 MHz at a level of 3.0 mV RMS

f. Verify that the EXT STD LED is lit and that the Channel A TRIG LED is flashing

g. Adjust R192 to obtain the most stable display indication of 100.0 E6 ± 0.1 E6, with the GATE LED flashing

NOTE:

Care is needed when adjusting R192. The display indication is random with R192 set to either side of the correct position.

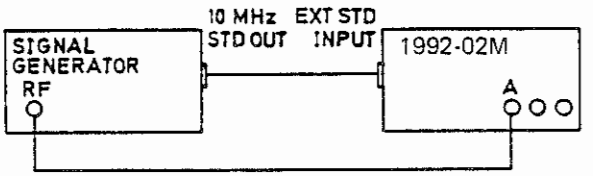


Figure 6.22 - Connections for Channel A Input System Adjustment

6.7.2.3 **Counter Test Procedure**

a. Switch off the RF output of the signal generator

b. Press the RESOLUTION ↑ key five times until 00000000 is displayed

c. Switch on the RF output of the signal generator

d. Increase the signal generator output to 13 mV RMS

e. Adjust R149 slowly clockwise until the display just becomes unstable. Turn back until the display is just stable and indicates 100.000000 E6 0.000001 E6

f. Reduce the signal generator output to 7 mV RMS. Verify that the GATE LED stops flashing. If it does not, repeat steps d to f

g. Switch off the counter. Disconnect the test equipment

6.7.3 Channel B Input System

6.7.3.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Coaxial Connecting Lead (Qty. 2)	7

6.7.3.2 Counter Setup Procedure

6.7.3.2.1 Set R150 fully counter-clockwise and R193 to its mid-position. R193 is located inside the screened module as shown in Figure 6.23.

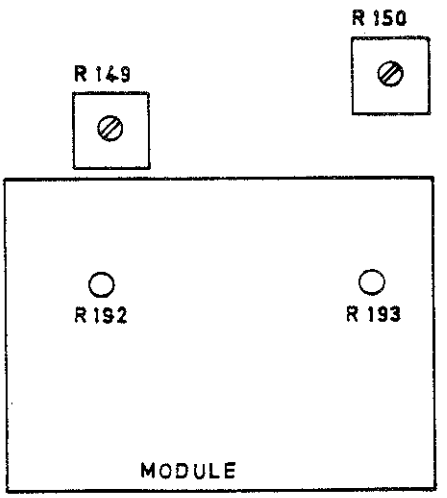


Figure 6.23 - Location of R150 and R193

6.7.3.2.2 Complete the following procedure:

a. Switch the 1992-02M on. Select FREQ A

b. Select 50Ω impedance for Channel B and press

[2] [1] [SHIFT] [STORE] [SF] [SHIFT] [SF]

c. Press the RESOLUTION ↓ key five times, until 000 is displayed

d. Connect the test equipment as shown in Figure 6.24

e. Set the signal generator output to 100 MHz at a level of 3.0 mV RMS

f. Verify that the EXT STD LED is lit and that the Channel B TRIG LED is flashing

g. Adjust R193 to obtain the most stable display indication of 100.0 E6 ± 0.1 E6, with the GATE LED flashing

NOTE:

Care is needed when adjusting R193. The display indication is random with R193 set to either side of the correct position.

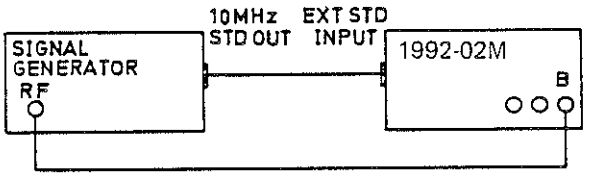


Figure 6.24 - Connections for Channel B Input System Adjustment

6.7.3.3 Counter Test Procedure

a. Switch off the RF output of the signal generator

b. Press the RESOLUTION ↑ key five times until 00000000 is displayed

c. Switch on the RF output of the signal generator

d. Increase the signal generator output to 13 mV RMS

e. Adjust R150 slowly clockwise until the display just becomes unstable. Turn back until the display is just stable and indicates 100.000000 E6 ± 0.000001 E6

f. Reduce the signal generator output to 7 mV RMS. Verify that the GATE stops flashing. If it does not, repeat steps d to f

g. Switch off the counter. Disconnect the test equipment

6.7.4 Channel C Assembly

6.7.4.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Coaxial Connecting Lead (Qty. 2)	7

6.7.4.1.1 Connect the test equipment as shown in Figure 6.25.

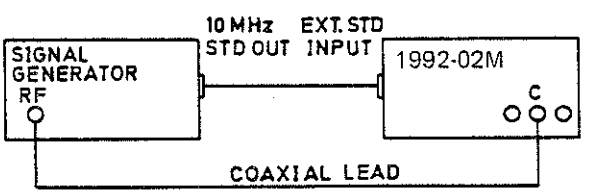


Figure 6.25 - Connections for Channel C Input System Adjustment

6.7.4.2 Counter Test Procedure

a. Set R27 on Channel C assembly fully clockwise

b. Switch the 1992-02M on. Select FREQ C. Verify that the EXT STD LED is lit

c. Set the signal generator output to 1 GHz at a level of 7.0 mV RMS

d. Adjust R27 until the gate LED just starts flashing and the counter display indicates 1000.00000 E6 ± 0.00001 E6

e. Switch the output of the signal generator off. Reduce the output level to 6.5 mV RMS

f. Switch the output of the signal generator on. Verify that the counter is not counting. If it is, repeat steps c to f

g. Switch off the counter. Disconnect the test equipment

6.8 INTERNAL FREQUENCY STANDARD - ROUTINE CALIBRATION

6.8.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Coaxial Connecting Lead	7

6.8.2 Calibration Procedure

a. Switch on the 1992-02M. Select FREQ A and verify that 00000000 is displayed and allow at least 72 hours of uninterrupted operation

b. Connect the test equipment as shown in Figure 6.26

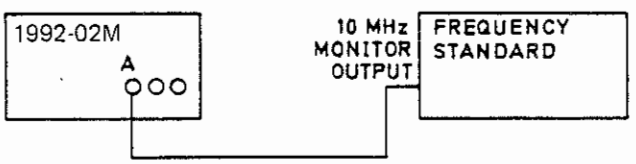


Figure 6.26 - Connections for Internal Frequency Standard Adjustment

c. Press [1] [0] [SHIFT] [EXP] [6] [SHIFT] [STORE] [X]

d. Press [SHIFT] [RECALL] [X]

Verify that 10.000000 E6 is displayed

e. Press [CONTINUE] and [SHIFT] [R-X/Z]

f. Adjust the internal frequency standard, via the aperture in the rear panel, to be as near to 10 MHz as possible. The display limits are shown in Table 6.3

g. Switch off the counter. Switch off and disconnect the test equipment

Table 6.3 - Internal Frequency Standard Accuracy

Frequency Standard	Display	Accuracy
04E Oscillator	±10 E-3	1 part in 10^9

6.9 OVERALL PERFORMANCE VERIFICATION PROCEDURE

6.9.1 Introduction

6.9.1.1 By correctly completing the following Performance Verification Procedures (PVPs), functional operation of the 1992-02M is verified. The primary purpose of these tests is to provide a relatively fast and easy method for determining the operability of the counter. These PVPs should be performed in the order given.

6.9.1.2 These PVPs should be performed whenever it is necessary to determine whether the 1992-02M is operating correctly. These tests may also be used as an incoming inspection procedure, or to verify a suspected failure. In addition, after diagnosing and repairing a 1992-02M failure, these PVPs can be used to confirm a satisfactory repair.

6.9.1.3 Before beginning the performance check, ensure that the counter satisfactorily passes the preliminary test given in Subsection 2.6 of this manual.

6.9.1.4 The following conditions must be maintained throughout the performance check:

a. The instrument must be operated from an AC supply

b. The line voltage must be within 10% of the value indicated by the line voltage selector

c. The instrument covers must be fitted

d. The ambient temperature must be $23^{\circ}C \pm 2^{\circ}C$

e. The power supply to the frequency standard must be uninterrupted

6.9.1.5 The instrument should be allowed to warm up for one hour (switched to standby, if required) before beginning the performance check.

6.9.2 Channel

6.9.2.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Digital Multimeter	3
Audio Oscillator	5
T-piece	8
Coaxial Connecting Lead (Qty. 2)	7

6.9.2.2 Channel A PVP (I)

a. Switch on the 1992-02M. Select 50Ω on Channel A

b. Connect the test equipment as shown in Figure 6.27. Check that the EXT STD LED lights

c. Set the signal generator output to the frequencies shown in Table 6.4 in turn. Set the counter's resolution to the corresponding value

d. At each frequency, determine the minimum input level to the counter which gives stable counting. Verify that this is not more than the level shown in Table 6.4

e. Disconnect the test equipment

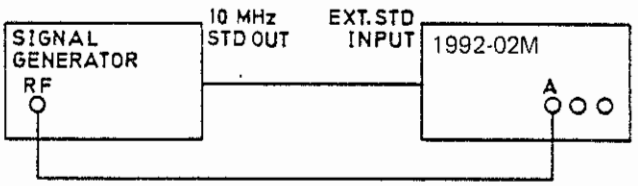


Figure 6.27 - Connections for Channel A Sensitivity PVP (I)

Table 6.4 - Channel A Sensitivity (I)

Frequency	1992-02M Resolution	Signal Level
160 MHz	8 digits	50 mV
100 MHz	8 digits	25 mV
10 MHz	7 digits	25 mV
100 kHz	5 digits	25 mV

6.9.2.3 Channel A PVP (II)

a. Connect the test equipment as shown in Figure 6.28

b. Set the signal generator output to the frequencies shown in Table 6.5 in turn. Set the counter's resolution to the corresponding value

c. At each frequency, determine the minimum input level to the counter which gives stable counting. Verify that this is not more than the level shown in Table 6.5

d. Disconnect the test equipment

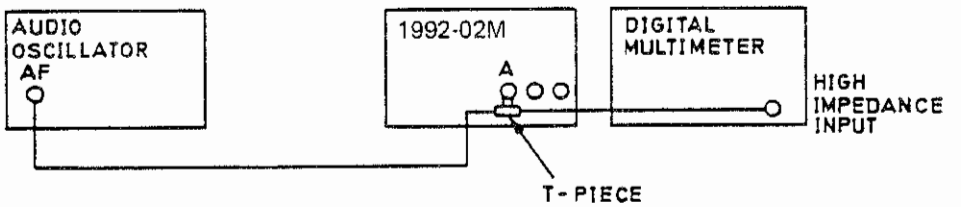


Figure 6.28 - Connections for Channel A Sensitivity PVP (II)

Table 6.5 - Channel A Sensitivity (II)

Frequency	1992-02M Resolution	Signal Level
5 kHz	3	25 mV
10 Hz	3	25 mV

6.9.3 Channel B Sensitivity PVP

6.9.3.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Signal Generator	1
Digital Multimeter	3
Audio Oscillator	5
T-piece	8
Coaxial Connecting Lead (Qty. 2)	7

6.9.3.2 Channel B PVP (I)

a. Select 50Ω on Channel B

b. Connect the test equipment as shown in Figure 6.29. Check that the EXT STD LED lights

c. Press [2] [1] [SHIFT] [STORE] [SF] [SHIFT] [SF]

d. Set the signal generator output to the frequencies shown in Table 6.6 in turn. Set the counter's resolution to the corresponding value

e. At each frequency, determine the minimum input level to the counter which gives stable counting. Verify that this is not more than the level shown in Table 6.6

f. Disconnect the test equipment

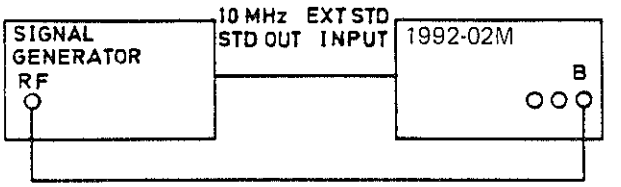


Figure 6.29 - Connections for Channel B Sensitivity PVP (I)

Table 6.6 - Channel B Sensitivity (I)

Frequency	1992-02M Resolution	Signal Level
100 MHz	8 digits	25 mV
10 MHz	7 digits	25 mV
100 kHz	5 digits	25 mV

6.9.3.3 Channel B PVP (II)

a. Connect the test equipment as shown in Figure 6.30

b. Set the signal generator output to the frequencies shown in Table 6.7 in turn. Set the counter's resolution to the corresponding value

c. At each frequency, determine the minimum input level to the counter which gives stable counting. Verify that this is not more than the level shown in Table 6.7

d. Press [2] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF]

e. Disconnect the test equipment

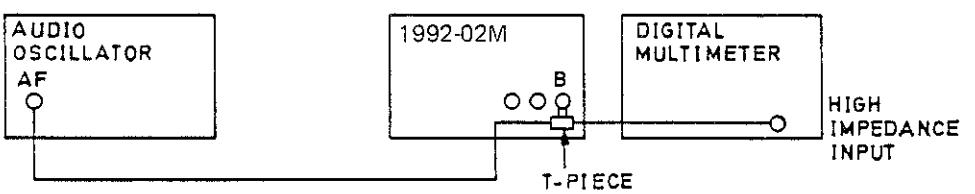


Figure 6.30 - Connections for Channel B Sensitivity PVP (II)

Table 6.7 - Channel B Sensitivity (II)

Frequency	1992-02M Resolution	Signal Level
5 kHz	3	25 mV
10 Hz	3	25 mV

6.9.4 Channel C Sensitivity PVP

6.9.4.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Coaxial Connecting Lead (Qty. 2)	7

6.9.4.2 Channel C PVP

a. Connect the test equipment as shown in Figure 6.31

b. Select FREQ C

c. Set the signal generator output to the frequencies shown in Table 6.8 in turn. Set the counter's resolution to the corresponding value

d. At each frequency, determine the minimum input level to the counter which gives stable counting. Verify that this is not more than the level shown in Table 6.8

e. Disconnect the test equipment

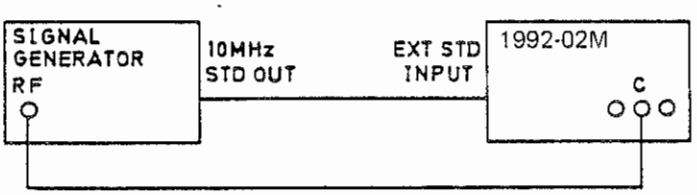


Figure 6.31 - Connections for Channel C Sensitivity PVP

Table 6.8 - Channel C Sensitivity

Frequency	1992-02M Resolution	Signal Level
40 MHz	8 digits	15 mV
100 MHz	8 digits	15 mV
500 MHz	8 digits	15 mV
1000 MHz	9 digits	15 mV
1300 MHz	9 digits	75 mV

6.9.5 External Standard Input Sensitivity PVP

6.9.5.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1

6.9.5.2 External Standard Input PVP

a. Connect the signal generator output to the EXT STD INPUT socket on the rear panel of the 1992-02M

b. Set the signal generator output to 10 MHz at a level of 10 mV RMS

c. Slowly increase the signal level until the counter's EXT STD LED lights steadily

d. Verify that the signal level is not more than 100 mV RMS

e. Disconnect the test equipment

6.9.6 10 MHz Standard Output Level PVP

6.9.6.1 Required Test Equipment

Item	Table 6.1, Item No.
Oscillator	2
T-piece	8
Load	9
Coaxial Connecting Lead	7

6.9.6.2 10 MHz Standard Output PVP

a. Connect the test equipment as shown in Figure 6.32

b. Verify that the peak-to-peak amplitude of the displayed waveform is greater than 600 mV into 50 ohms. Verify that the mark/space ratio is between 30:70 and 70:30

c. Disconnect the test equipment

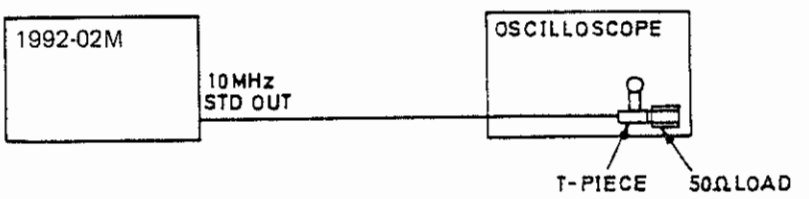


Figure 6.32 - Connections for 10 MHz Standard Output Level PVP

6.9.7 Minimum Time Interval PVP

6.9.7.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1

6.9.7.2

a. Connect the test equipment as shown in Figure 6.33

b. Select 50Ω on Channel A, T.I. A→B, and COM A

c. Set the signal generator output to 100 MHz at a level of 1V

d. Verify that a display of 0 ± 2ns is obtained

e. Disconnect the test equipment

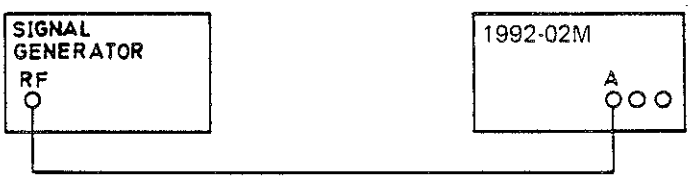


Figure 6.33 - Connections for Minimum Time Interval PVP

6.9.8 External Arming PVP

6.9.8.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Pulse Generator	6
Coaxial Connecting Lead (Qty. 3)	7

6.9.8.2

a. Select 50Ω on Channel A and FREQ A. Press the RESOLUTION ↓ key three times until 00000 is displayed

b. Connect the test equipment as shown in Figure 6.34

c. Set the signal generator output to 10 MHz at a level of 200 mVRMS

d. Prepare the pulse generator to give a single, 300 μs, positive-going pulse with a low level of +0.4V and a high level of +2.4V (TTL limit levels)

e. Press [1] [6] [SHIFT] [STORE] [SF] [SHIFT] [SF]

f. Verify that the instrument is not counting

g. Trigger the pulse generator to obtain a single pulse output

h. Verify that the display indicates 10.0000 E6 Hz ±1 count and that the instrument is not continuously gating

i. Press [1] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF]

j. Disconnect the test equipment

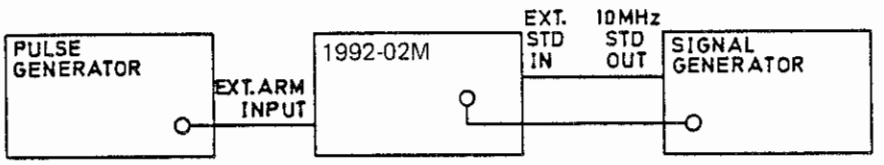


Figure 6.34 - Connections for External Arming PVP

6.9.9 Trigger Level PVP

6.9.9.1 Required Test Equipment

Item	Table 6.1, Item No.
Oscilloscope with Probe	2
Digital Multimeter	3

6.9.9.2 Trigger Level PVP (1)

a. Connect the test equipment as shown in Figure 6.35

b. Select DC coupling of the oscilloscope input

c. Set the oscilloscope to monitor a waveform of approximately 12V peak-to-peak with a frequency of approximately 2 Hz

d. Select CHECK

e. Press [7] [6] [SHIFT] [STORE] [SF] [SHIFT] [SF]

f. Verify that the Channel A and B TRIG LEDs are flashing and that the displayed waveform is as shown in Figure 6.36

g. Transfer the oscilloscope probe to the Channel B TRIG LEVEL OUTPUT pin and verify that the same waveform is displayed

h. Press [7] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF]

i. Disconnect the test equipment

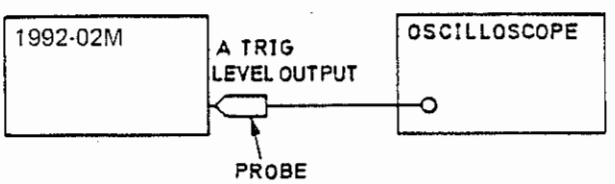


Figure 6.35 - Connections for Trigger Level PVP (1)

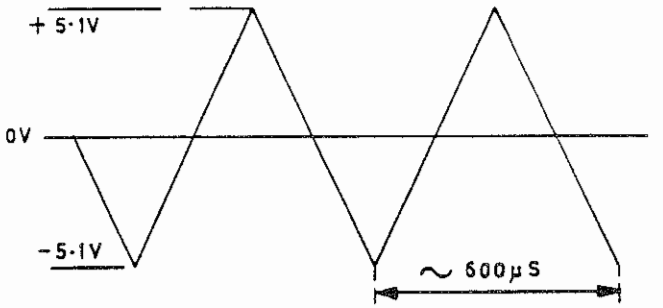


Figure 6.36 - Trigger Level Waveform

6.9.9.3 Trigger Level PVP (II)

a. Connect the test equipment as shown in Figure 6.37

b. Set the multimeter to measure DC volts

c. Press [TRIG LEVEL] [5] [TRIG LEVEL] on Channels A and B

d. Verify that the multimeter indicates +5V ± 60 mV

e. Transfer the probe to the Channel B TRIG LEVEL OUTPUT pin and verify that the multimeter indicates +5V ± 60 mV

f. Press [TRIG LEVEL] [0] [TRIG LEVEL] on Channels A and B

g. Verify that the multimeter indicates 0V ± 10 mV

h. Transfer the probe to the Channel A TRIG LEVEL OUTPUT pin and verify that the multimeter indicates 0V ± 10 mV

i. Press [TRIG LEVEL] [5] [SHIFT] [±] [TRIG LEVEL]

j. Verify that the multimeter indicates -5V ± 60 mV

k. Transfer the probe to the Channel B TRIG LEVEL OUTPUT pin and verify that the multimeter indicates -5V ± 60 mV

l. Disconnect the test equipment

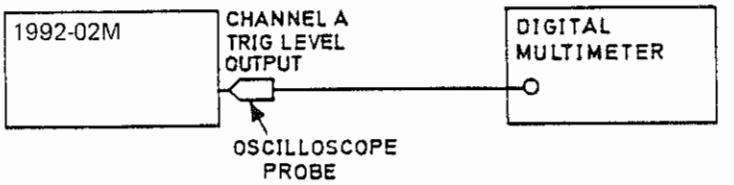


Figure 6.37 - Connections for Trigger Level PVP (II)

6.9.10 Internal Frequency Standard PVP

6.9.10.1 Required Test Equipment

Item	Table 6.1, Item No.
Frequency Standard	4
Coaxial Connecting Lead	7

6.9.10.2

a. Switch on the 1992-02M. Select FREQ A and verify that 00000000 is displayed. Allow 72 hours of uninterrupted operation

b. Connect the test equipment as shown in Figure 6.38

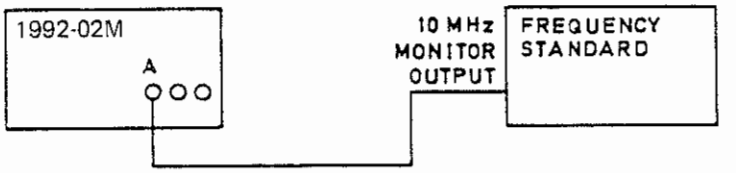


Figure 6.38 - Connections for Internal Frequency Standard PVP

c. Press [1] [0] [SHIFT] [EXP] [6] [SHIFT] [STORE] [X]

d. Press [SHIFT] [RECALL] [X]
Verify that 10.000000 E6 is displayed

e. Press [CONTINUE] and [SHIFT] [R-X/Z]

f. Verify that the value displayed is within the limits shown in Table 6.9

g. Switch off the 1992-02M. Switch off and disconnect the test equipment

Table 6.9 - Internal Frequency Standard Accuracy

Frequency Standard	Display	Accuracy
Oscillator 04E	±10 E-3	1 part in 10^9

SECTION 7 DRAWINGS

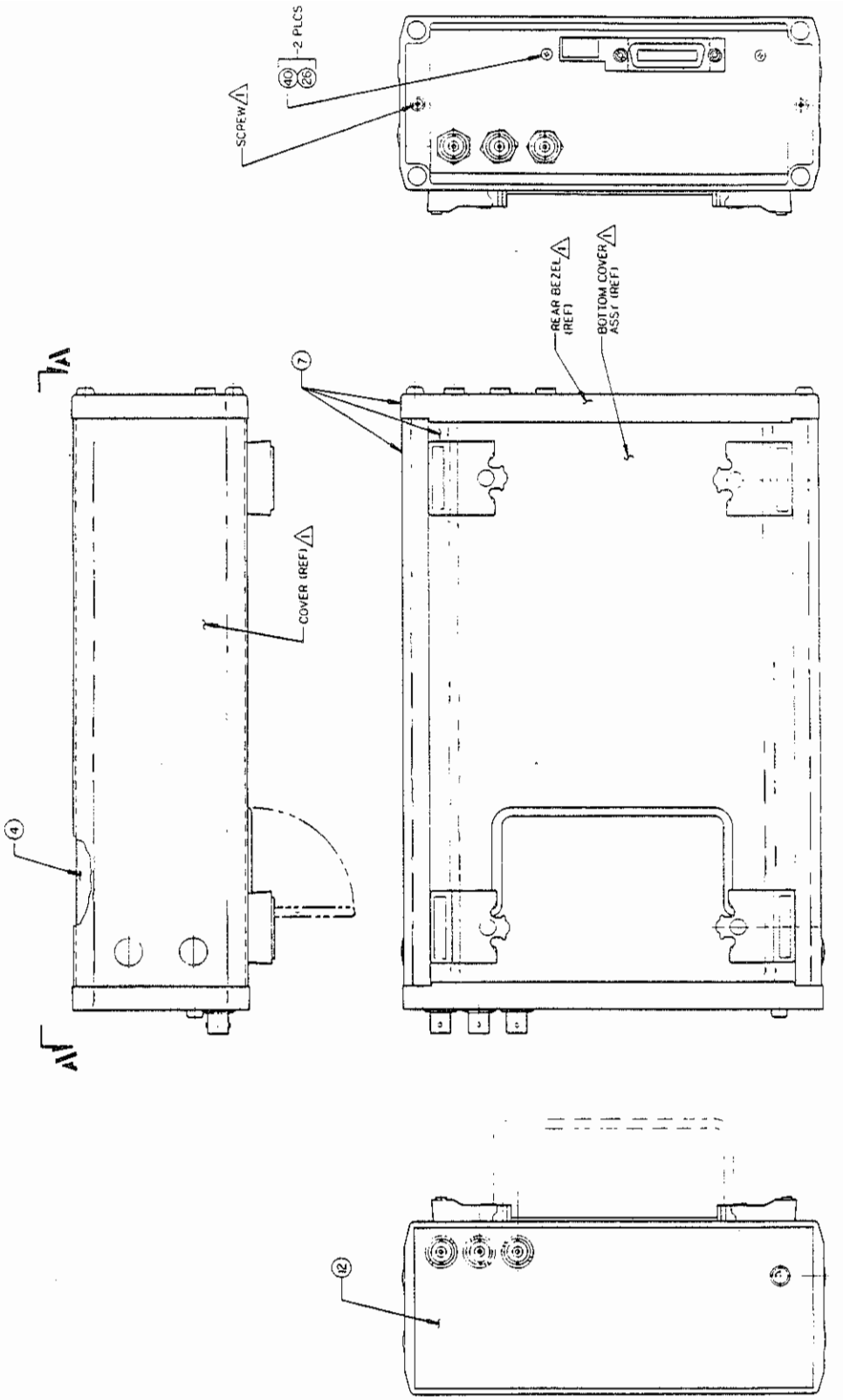


Figure 7.1A – Final Assembly (404503)

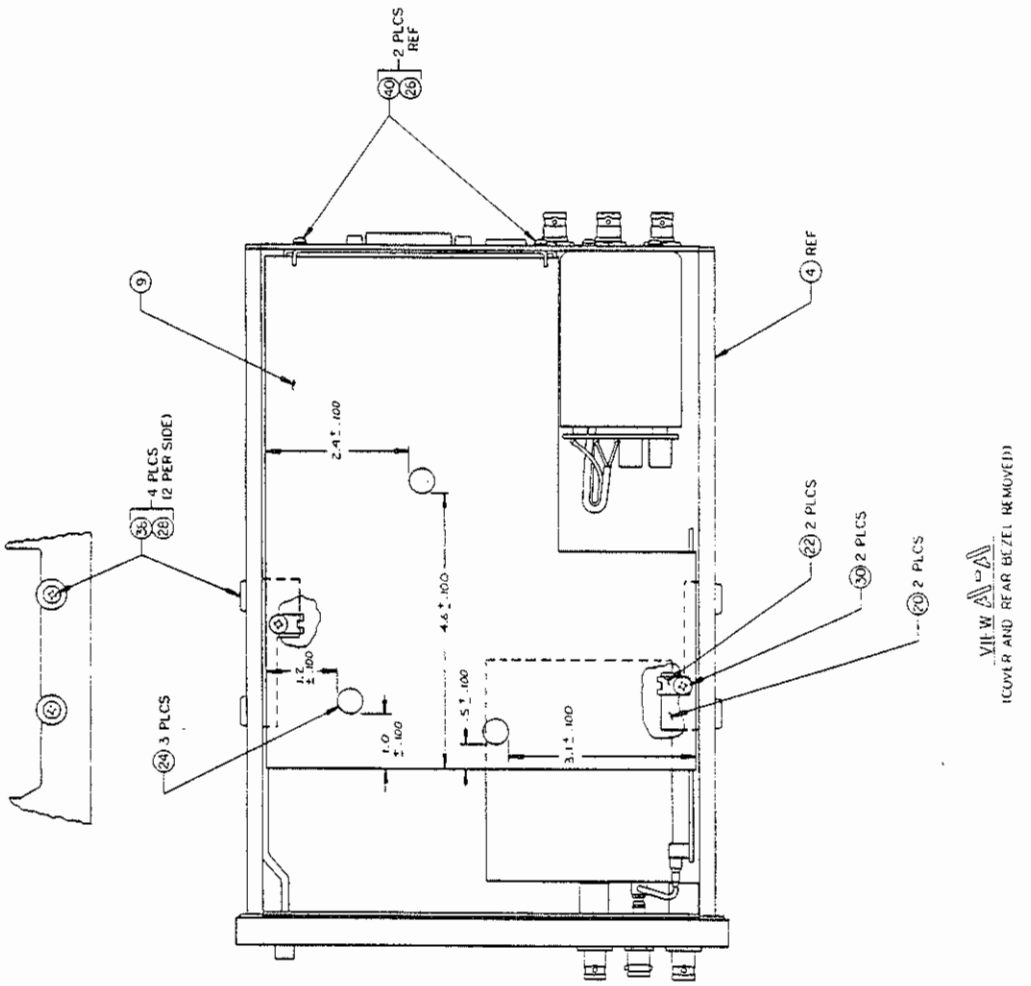


Figure 7.1A - Final Assembly (404503) (Cont'd)

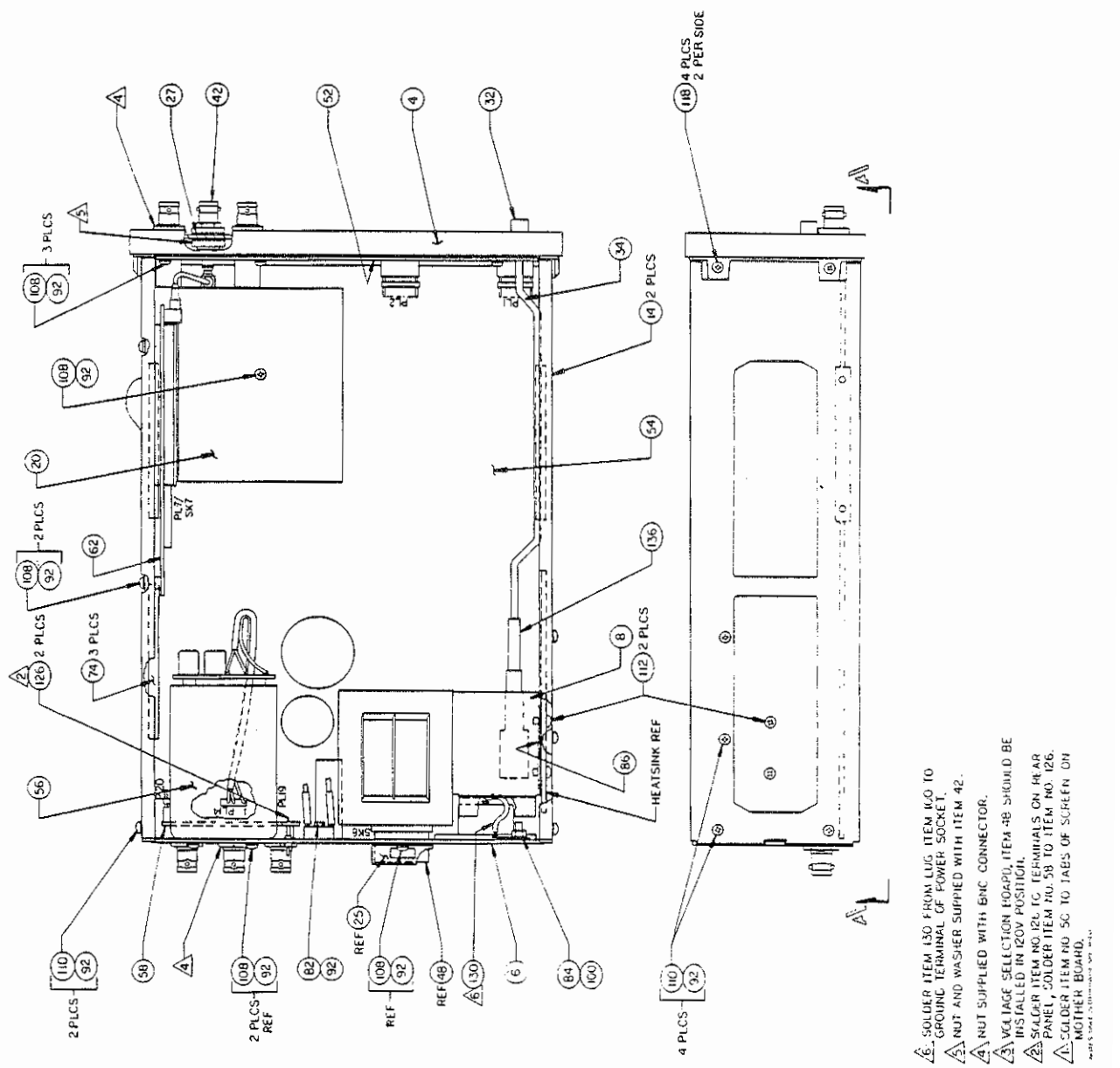


Figure 7.1B - Chassis Assembly (404506)

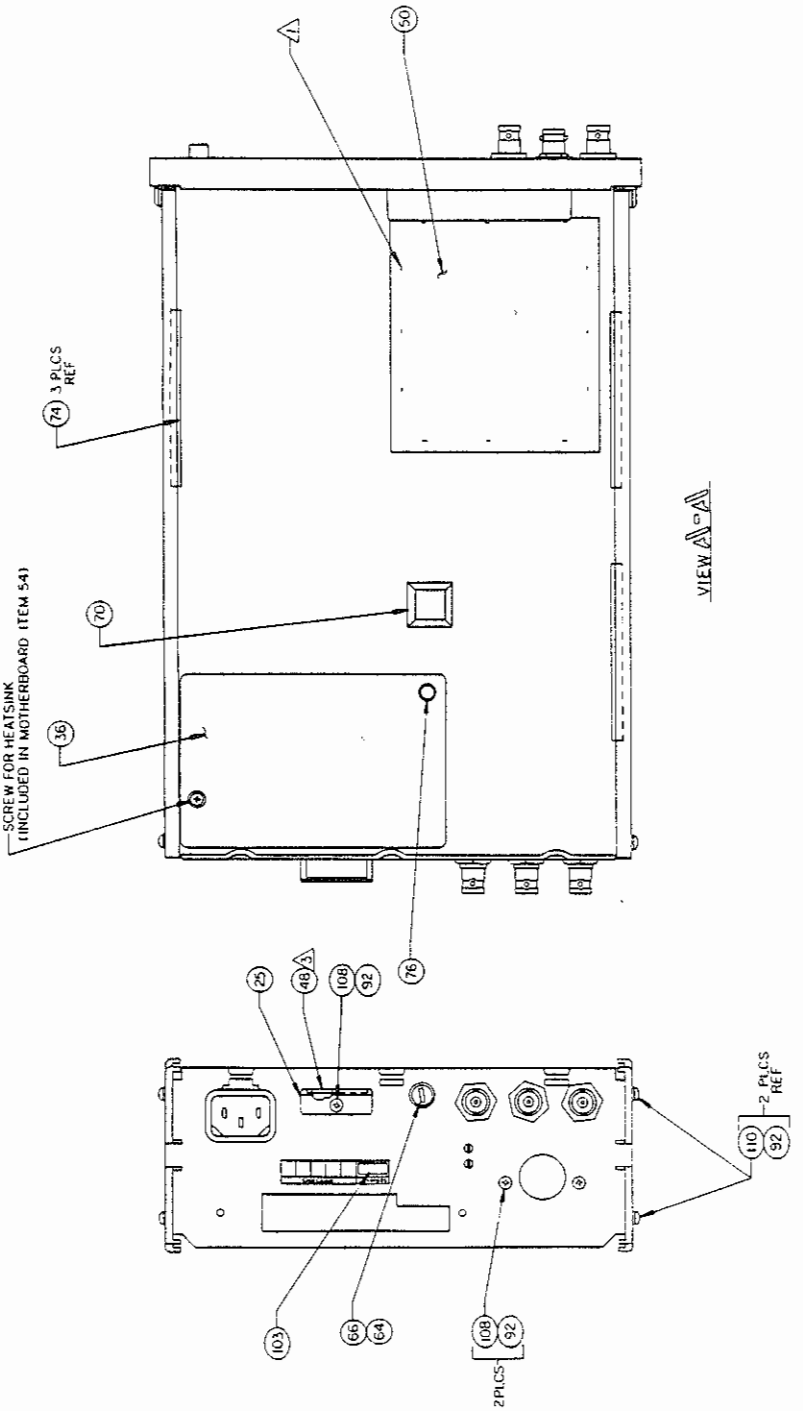


Figure 7.1B – Chassis Assembly (404506) (Cont'd)

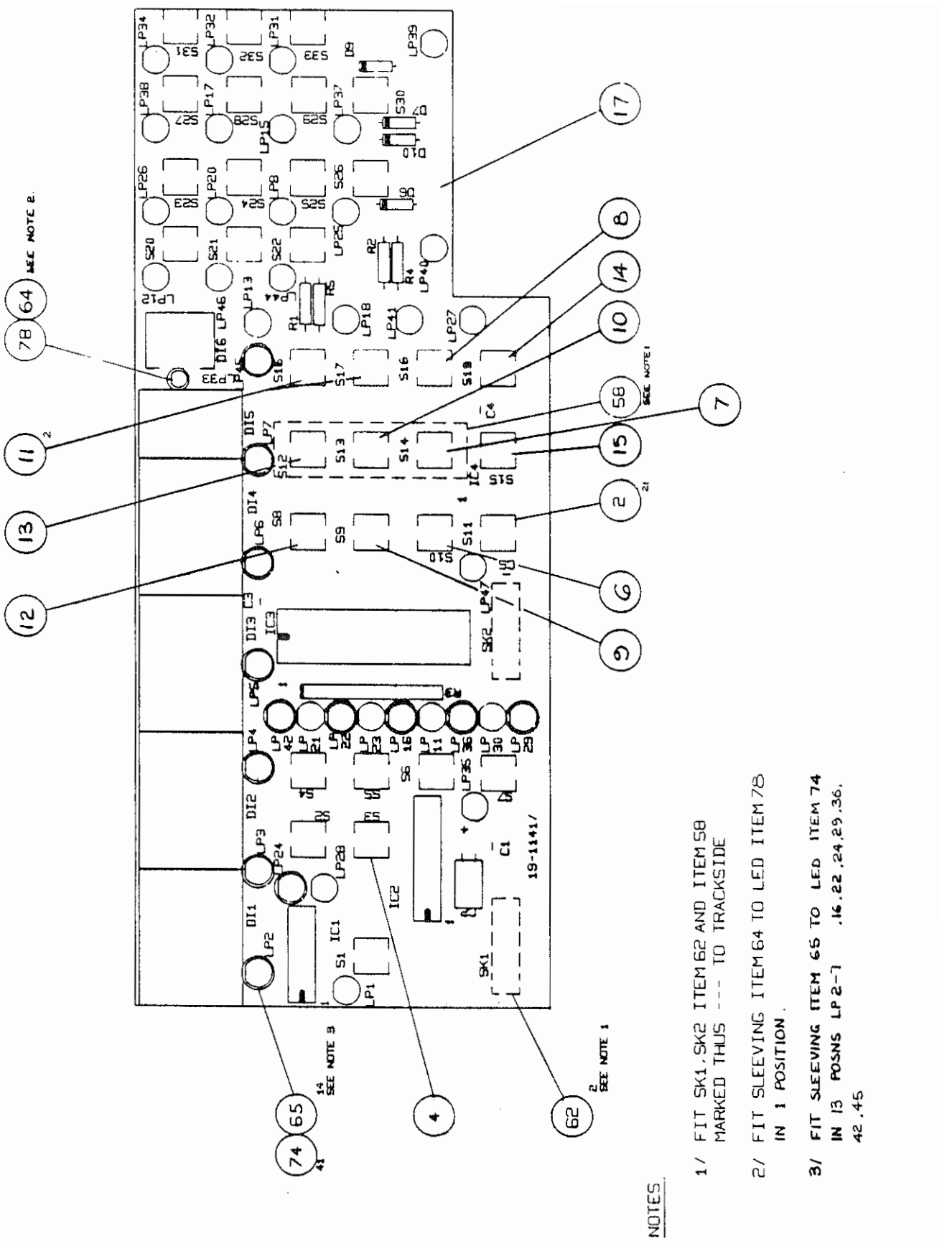


Figure 7.2 - Component Layout, Display (19-1141)

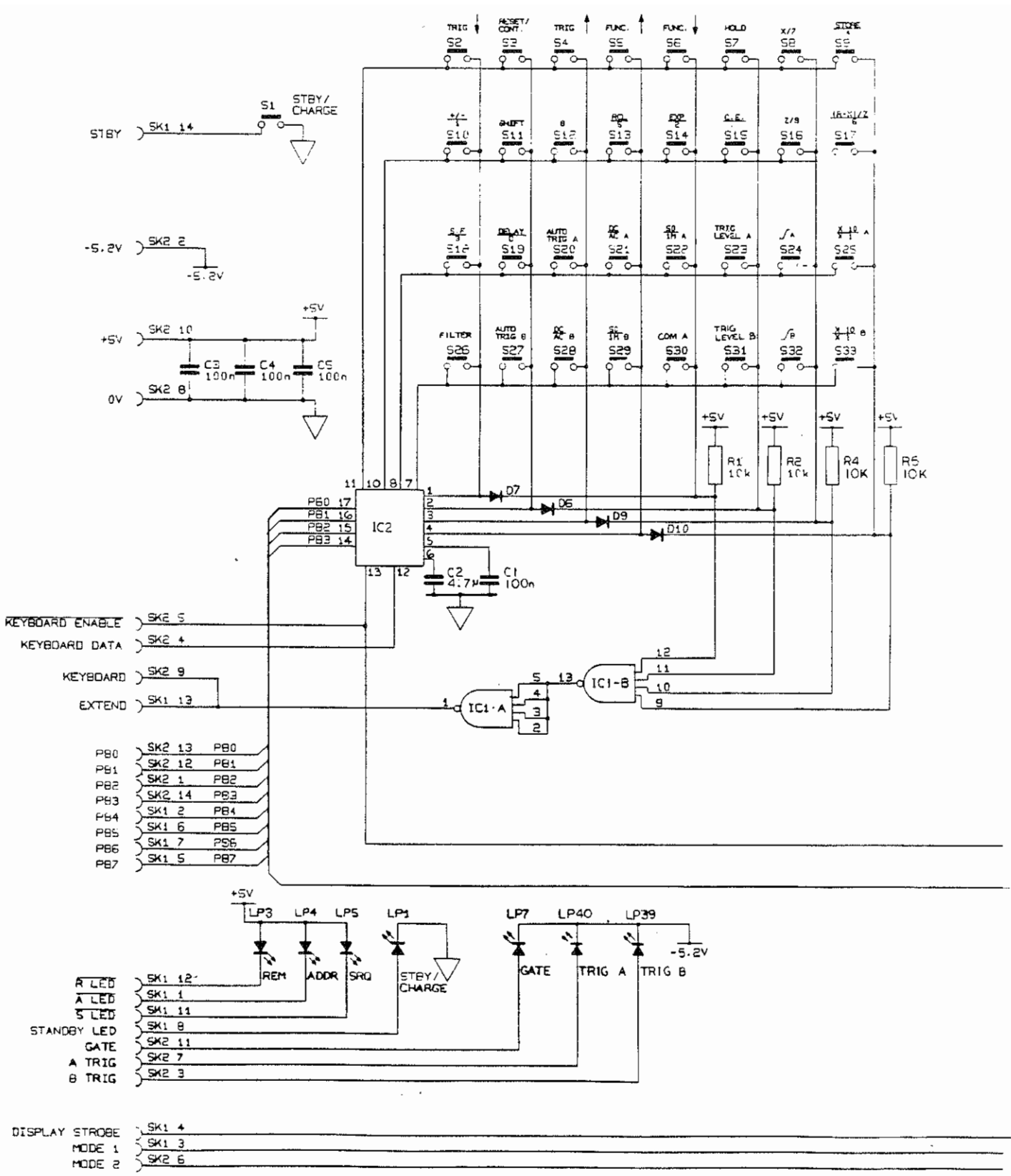
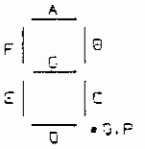


Figure 7.3 - Circuit Diagram, Display

REFERENCE	TYPE NO.	PART NO.	+5V	0V
D5,7,9,10	IN4149	R-22-1029		
IC1	4012	R-22-4754	14	7
IC3,4	7219AIJI	2.50457	19	26
IC2	74C922	R-22-4779	18	9
DI5	HD1109	R-26-1511		
DI1-4	MAN6910	R-26-1512		
DI5	MAN6960	R-26-1513		
LP33	LED RED	R-26-5018		
LP1-8,11-13	LED RED	R-26-5026		
15-16,20-32				
34-42,44-47				

COMPONENT REFERENCE	
R1-5	LP1-8,11-13
C1-5	15-18,20-42
D6,7,9,10	44-47
IC1-4	
DI1-6	
S1-33	
SK1,2	



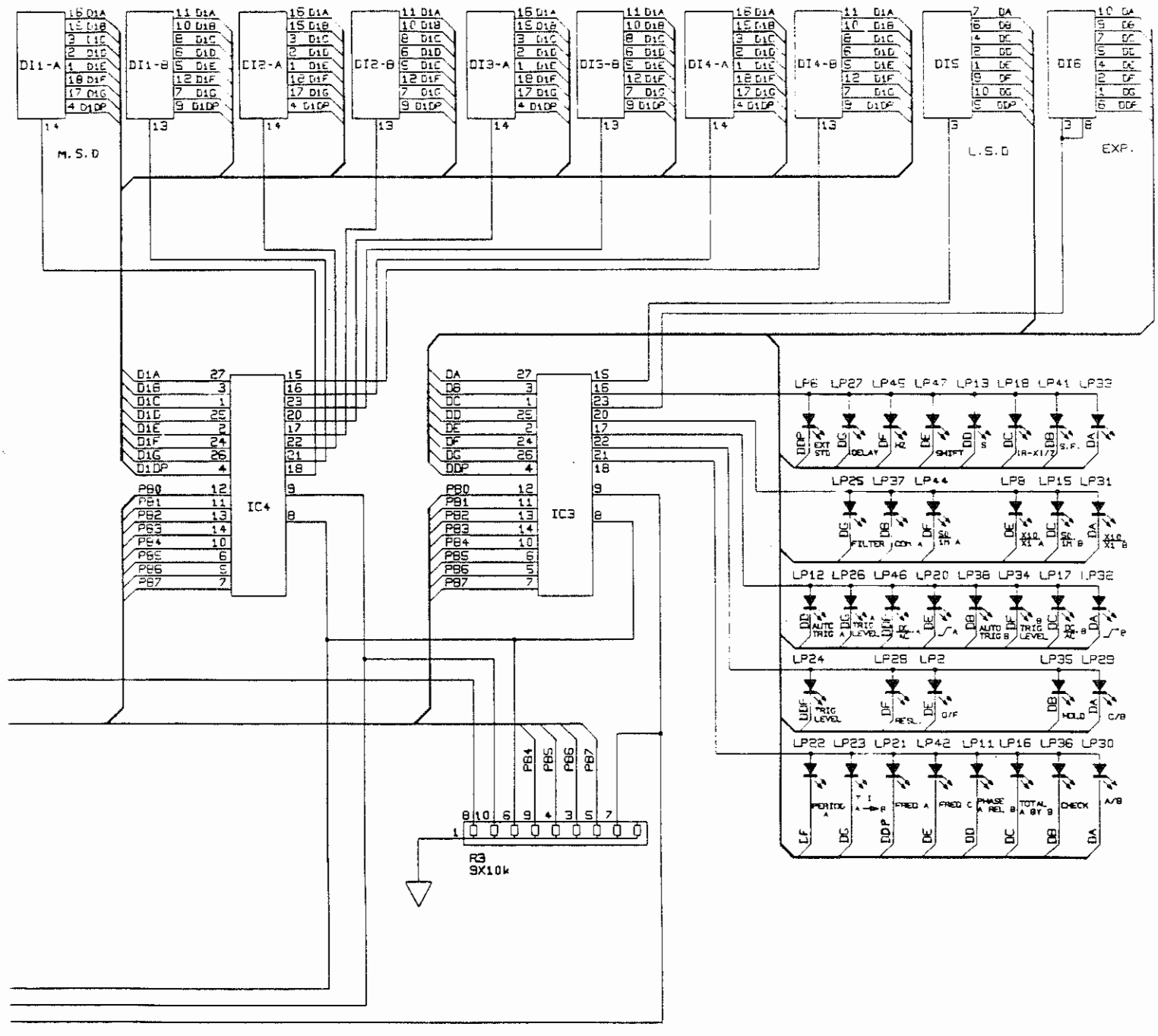


Figure 7.3 - Circuit Diagram, Display (Cont'd)

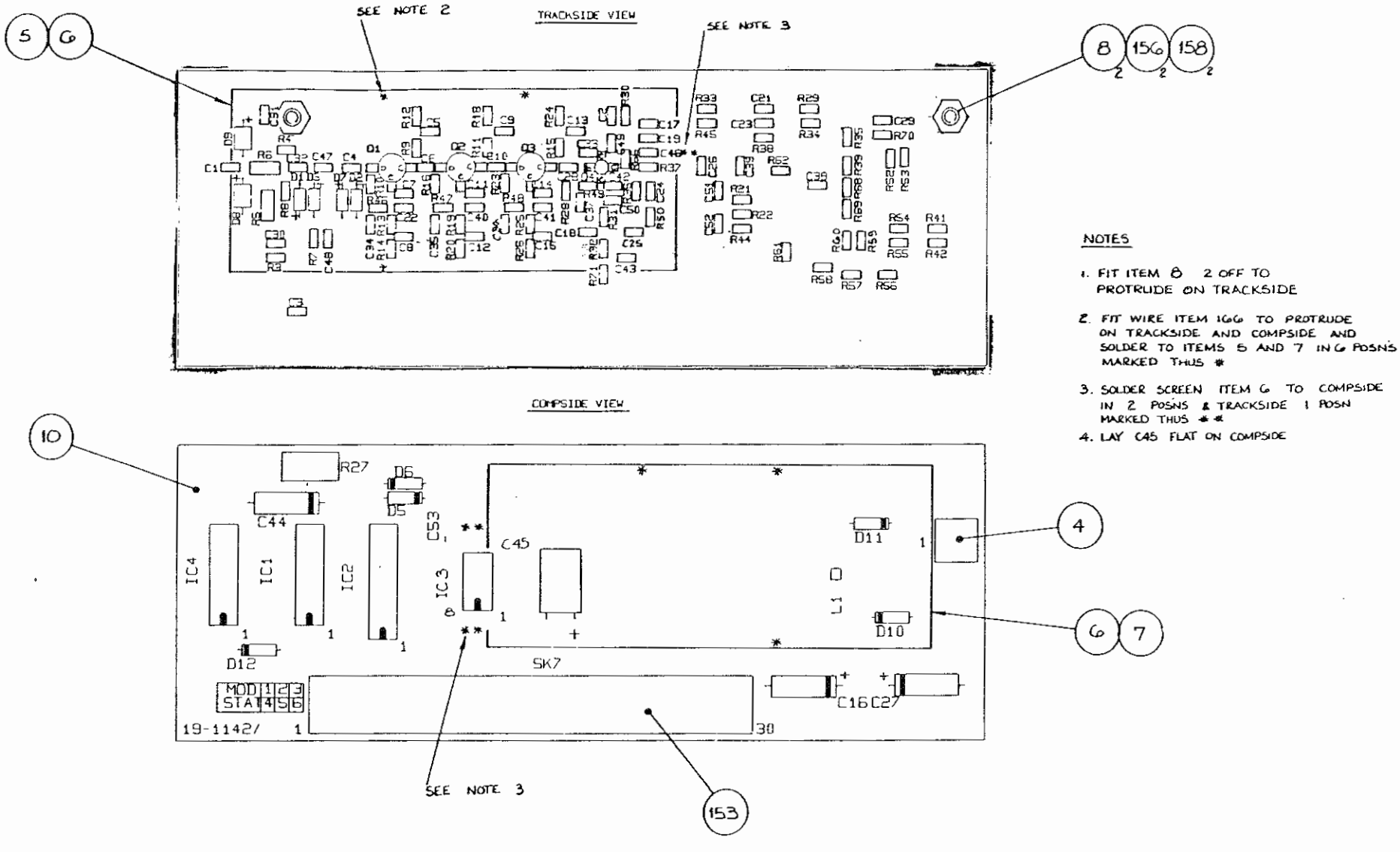


Figure 7.4 – Component Layout, Channel C (19-1142)

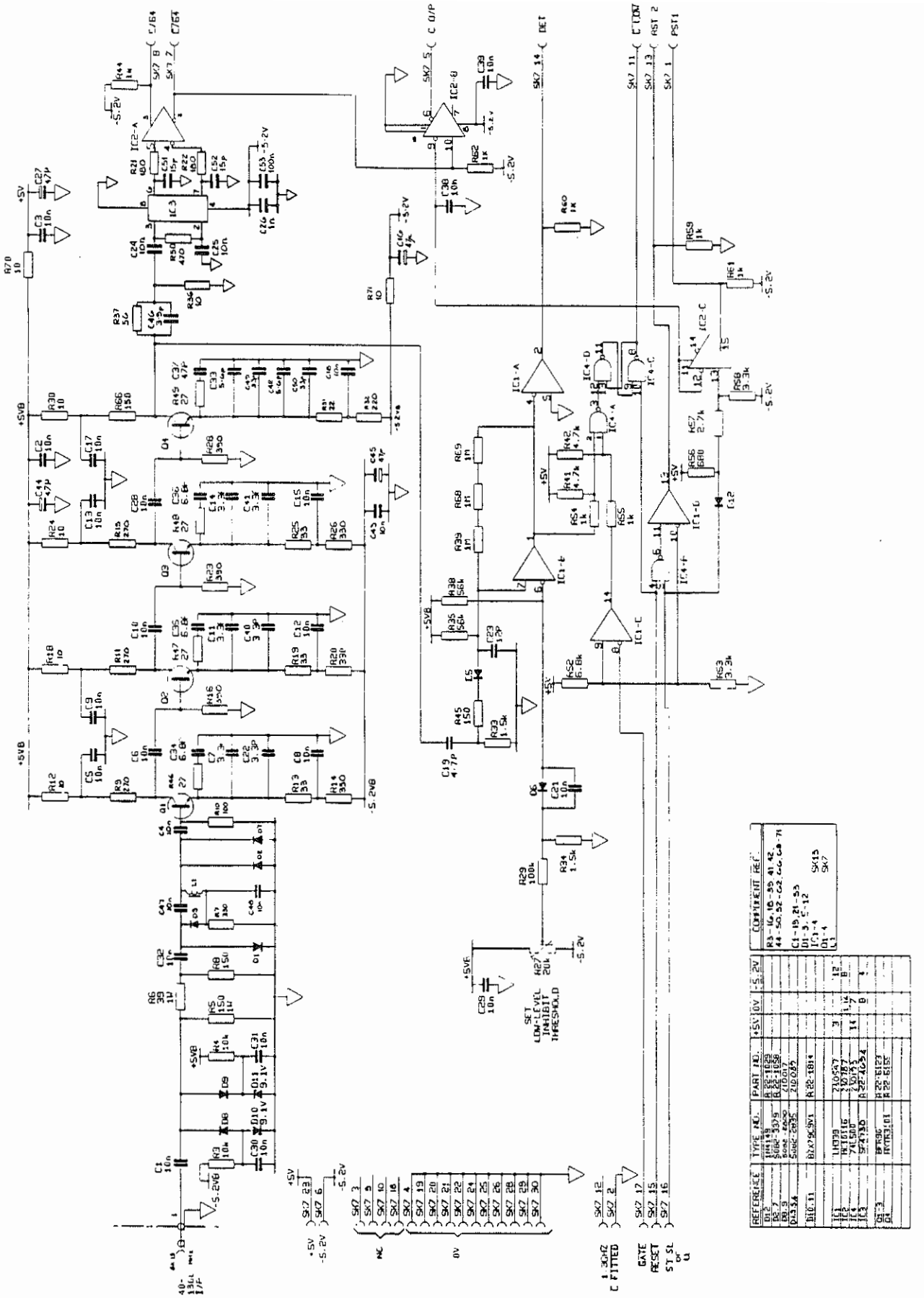
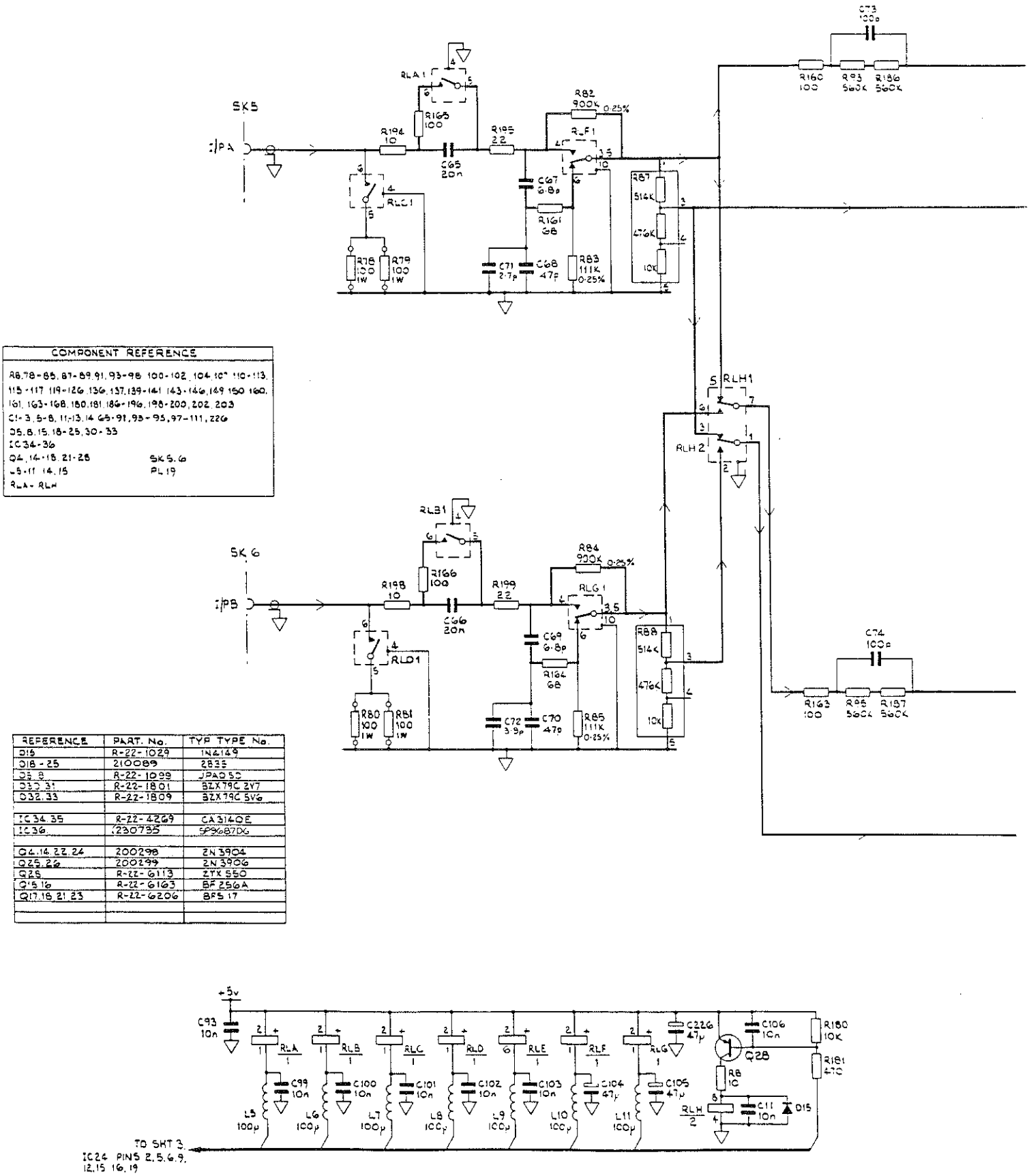


Figure 7.5 - Circuit Diagram, Channel C



COMPONENT REFERENCE	
R8,78-85,87-89,91,93-98 100-102 104,107 110-113, 115-117 119-126 136,137,139-141 143-146,149 150 160, 161, 163-168, 180,181,186-196, 198-200, 202, 203	
C1-3, 5-8, 11-13, 14 65-91, 93-95, 97-111, 226	
D5,8,15,18-25,30-33	
IC34-36	
Q4,14-18,21-28	SK5,6
L5-11 14,15	PL19
RLA-RLH	

REFERENCE	PART. No.	TYP TYPE No.
D15	R-22-1029	1N4149
D18-25	210089	2833
D5,8	R-22-1099	JPAD50
D30,31	R-22-1801	BZX79C 2V7
D32,33	R-22-1809	BZX79C 5V6
IC34,35	R-22-4269	CA3140E
IC36	230735	SP9687DG
Q4,14,22,24	200298	2N3904
Q25,26	200299	2N3906
Q25	R-22-6113	ZTX550
Q15,16	R-22-6163	BF256A
Q17,18,21,23	R-22-6206	BFS17

 Figure 7.7 – Circuit Diagram, Motherboard

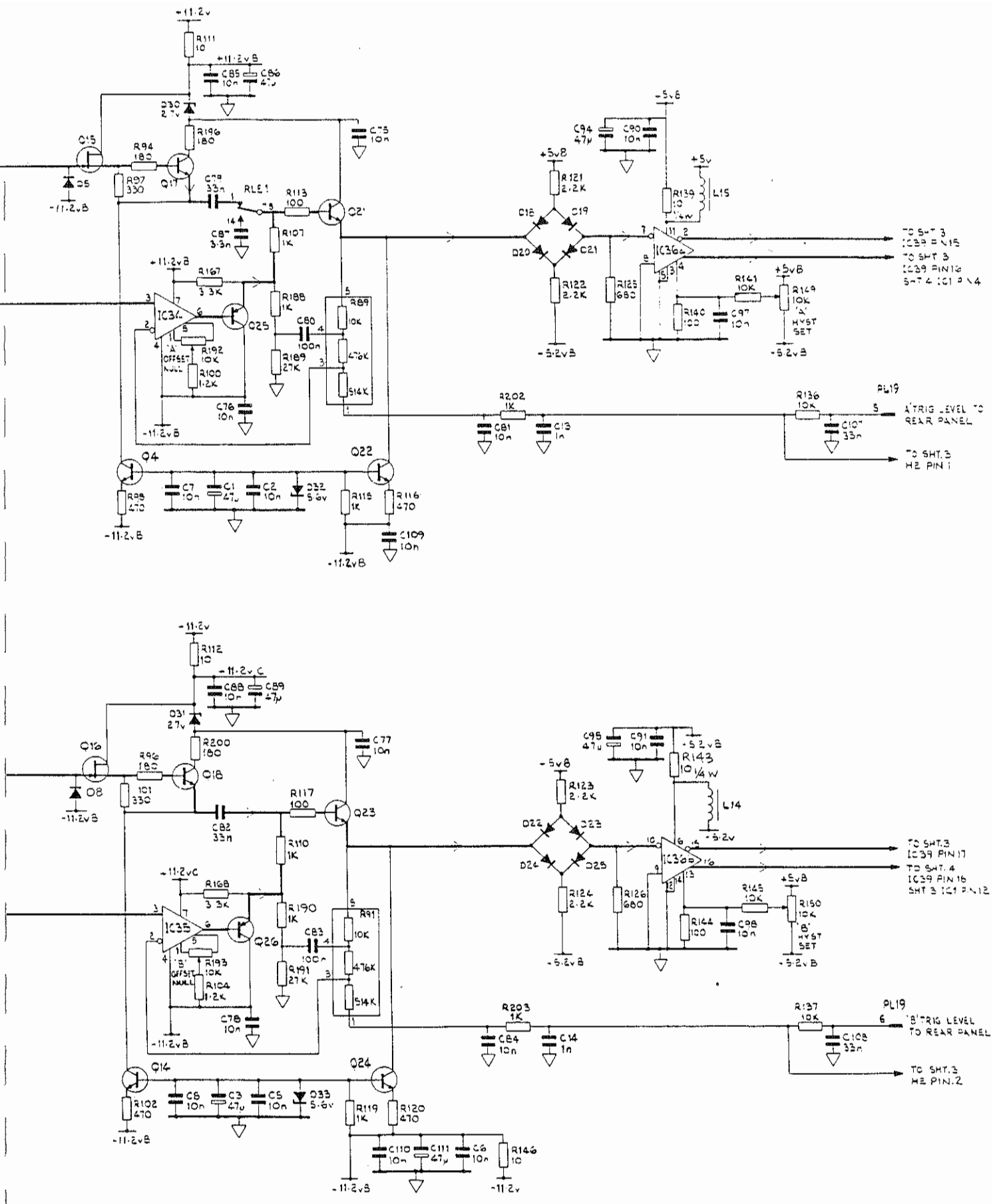
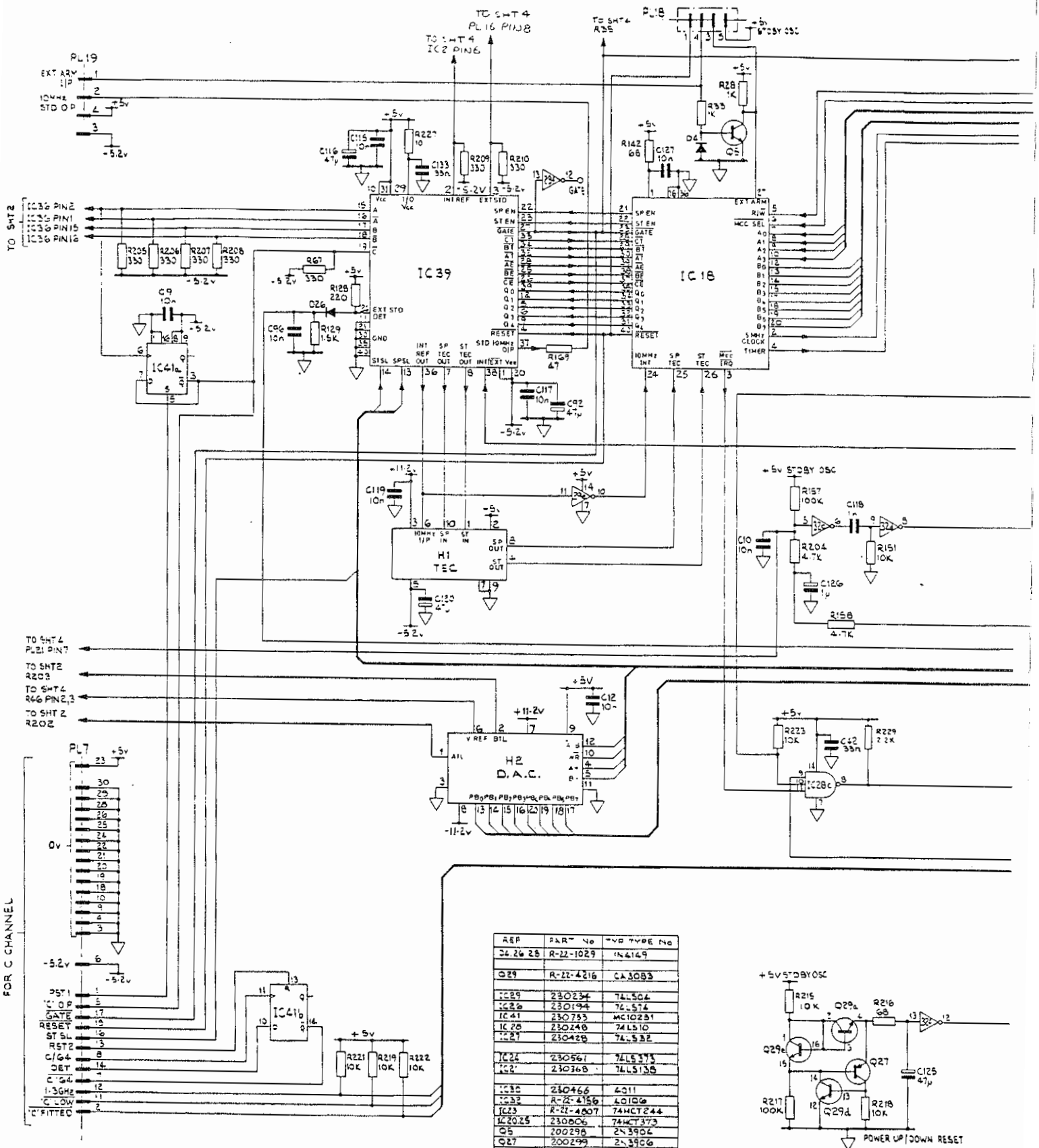


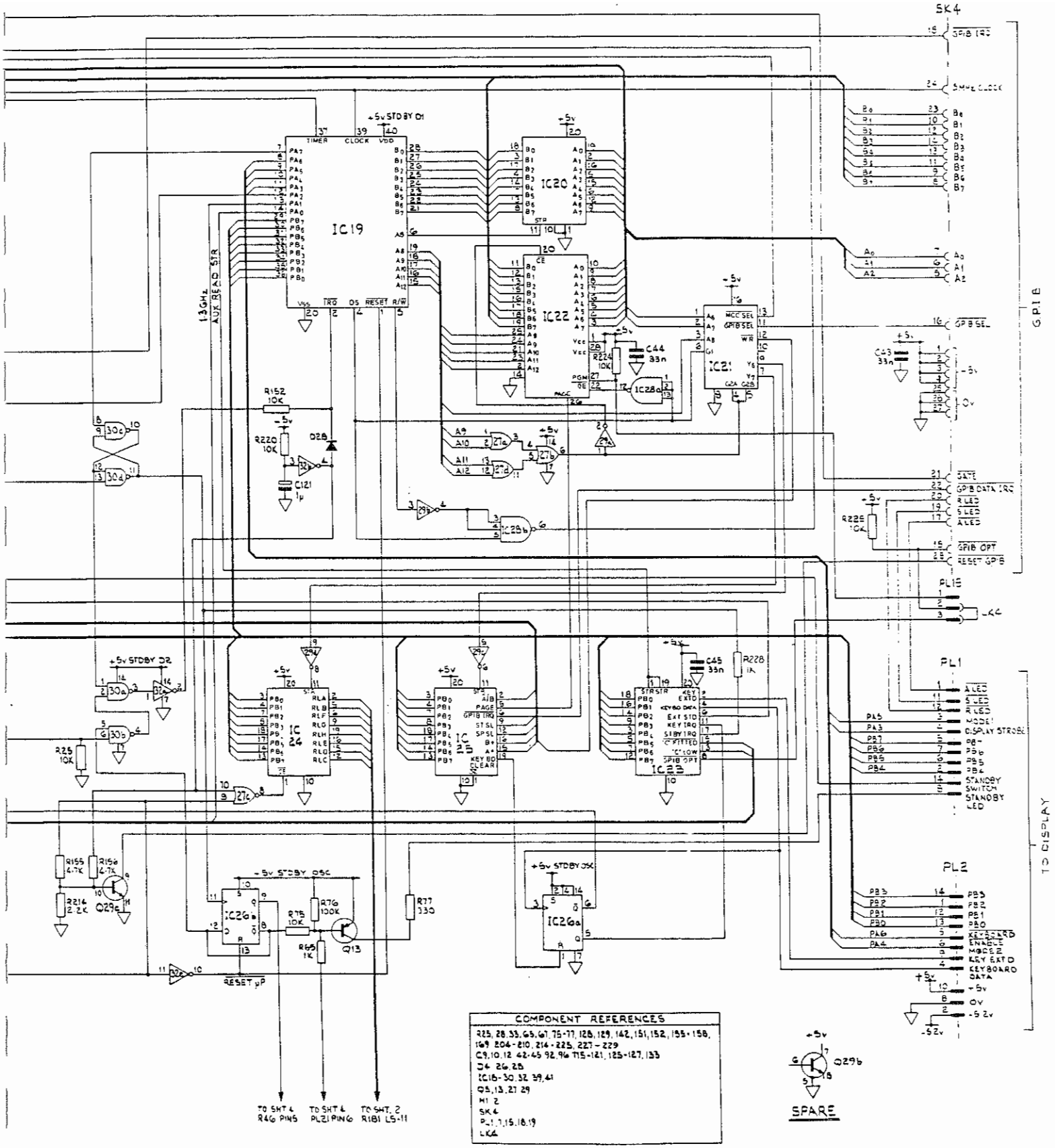
Figure 7.7 - Circuit Diagram, Motherboard (Cont'd)



REF	PART No	EYE TYPE No
D6,26,28	R-22-1029	IN4149
Q29	R-22-4216	CA3083
IC29	230234	74LS04
IC26	230194	74LS74
IC41	230753	MC10231
IC28	230248	74LS10
IC27	230428	74LS32
IC24	230561	74LS393
IC21	230368	74LS138
IC30	230466	4011
IC32	R-22-4156	40106
IC23	R-22-4007	74HCT244
IC20,25	230006	74HCT373
Q5	200298	2N3904
Q27	200299	2N3906
Q13	R-22-6113	ZTX550
IC19	R-22-8307	1466805E2
IC18	230790	MCC1
IC39	230789	MCC2
IC22	230867	27128

Figure 7.8 - Circuit Diagram, Motherboard

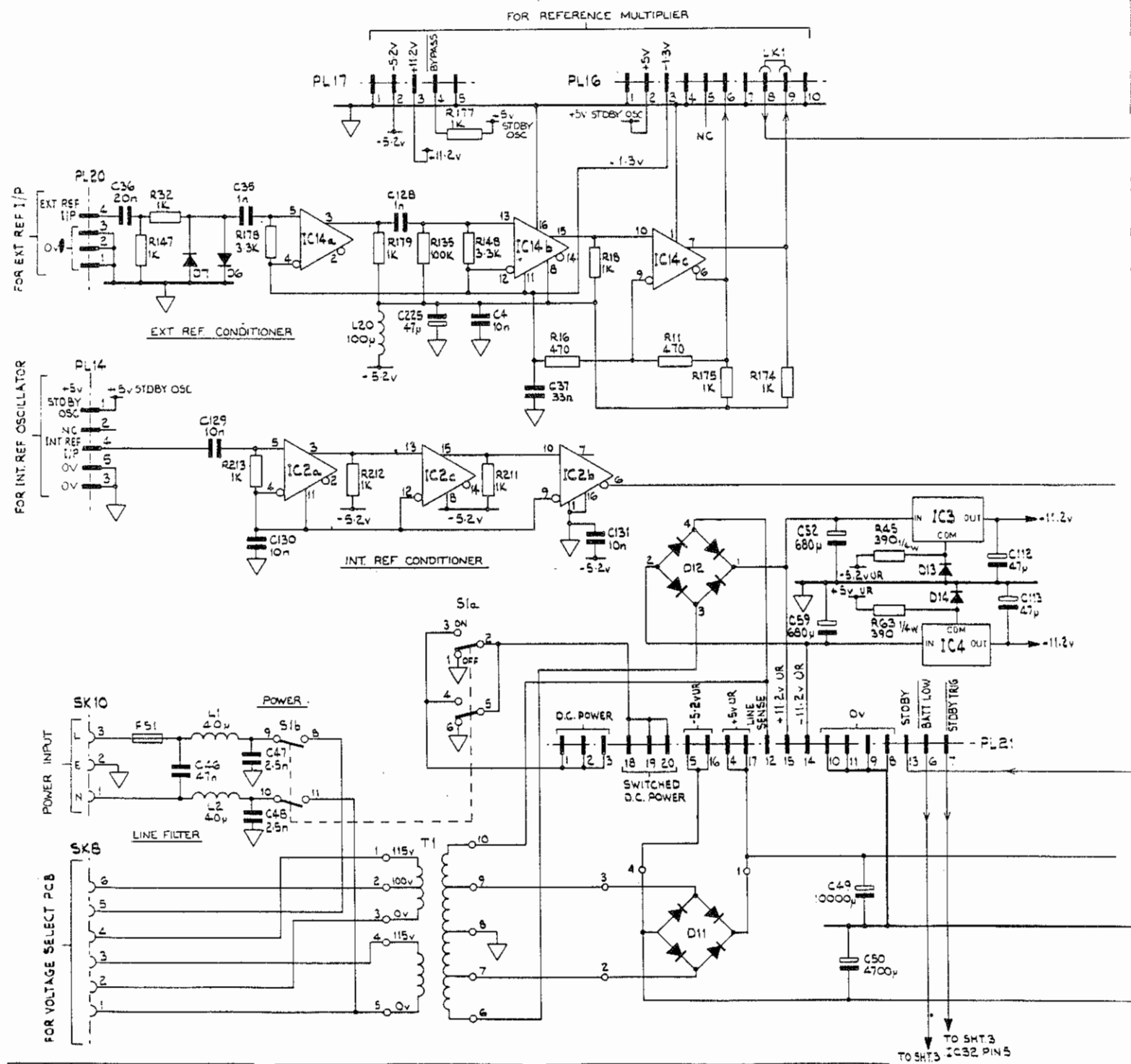
REV. D



COMPONENT REFERENCES

R25, 28, 33, 65, 67, 75-77, 128, 129, 142, 151, 152, 155-158, 169, 204-210, 214-225, 227-229
Q9, 10, 12, 42-45, 92, 96, 115-121, 125-127, 133
D4, 26, 28
IC18-30, 32, 39, 41
Q3, 13, 27, 29
H1, 2
SK4
PL1, 7, 15, 18, 19
LK4

Figure 7.8 – Circuit Diagram, Motherboard (Cont'd)



REF	PART No	TYP TYPE No
D1-3,6,7,13,14	R-22-1029	1N4149
D4	R-22-1662	VH248
D12	R-22-1664	B40C800
IC3	230200	7812CT
IC31	R-22-4262	MC3403
IC4	230201	7912CT
IC2,14	230787	10116
IC1	230750	10216

REF	PART No	TYP TYPE No.
Q11	200298	2N3904
Q1-3	R-22-6018	MPS3640
Q9,10	R-22-6112	ZTX450
Q7	R-22-6113	ZTX550
Q6	200302	BDT91
Q8,12	200301	BDT92

COMPONENT REFERENCE	
R1-7, 11, 16, 18, 32, 35, 40, 45-49, 54, 60, 63, 68, 135, 147, 148, 159, 170, 171, 174, 175, 177-179, 211-213, 226	
C4, 22-28, 35-37, 40, 41, 46-50, 52-59, 112-114, 128-132, 225.	
D1-3, 6, 7, 11-14.	FS1
IC1-4, 14, 31	S1 LK1
Q1-3, 6-12	T1
L1, 2, 20.	SK8, 10
	PL2, 14, 16, 17, 20, 21.

REV. D

Figure 7.9 - Circuit Diagram, Motherboard

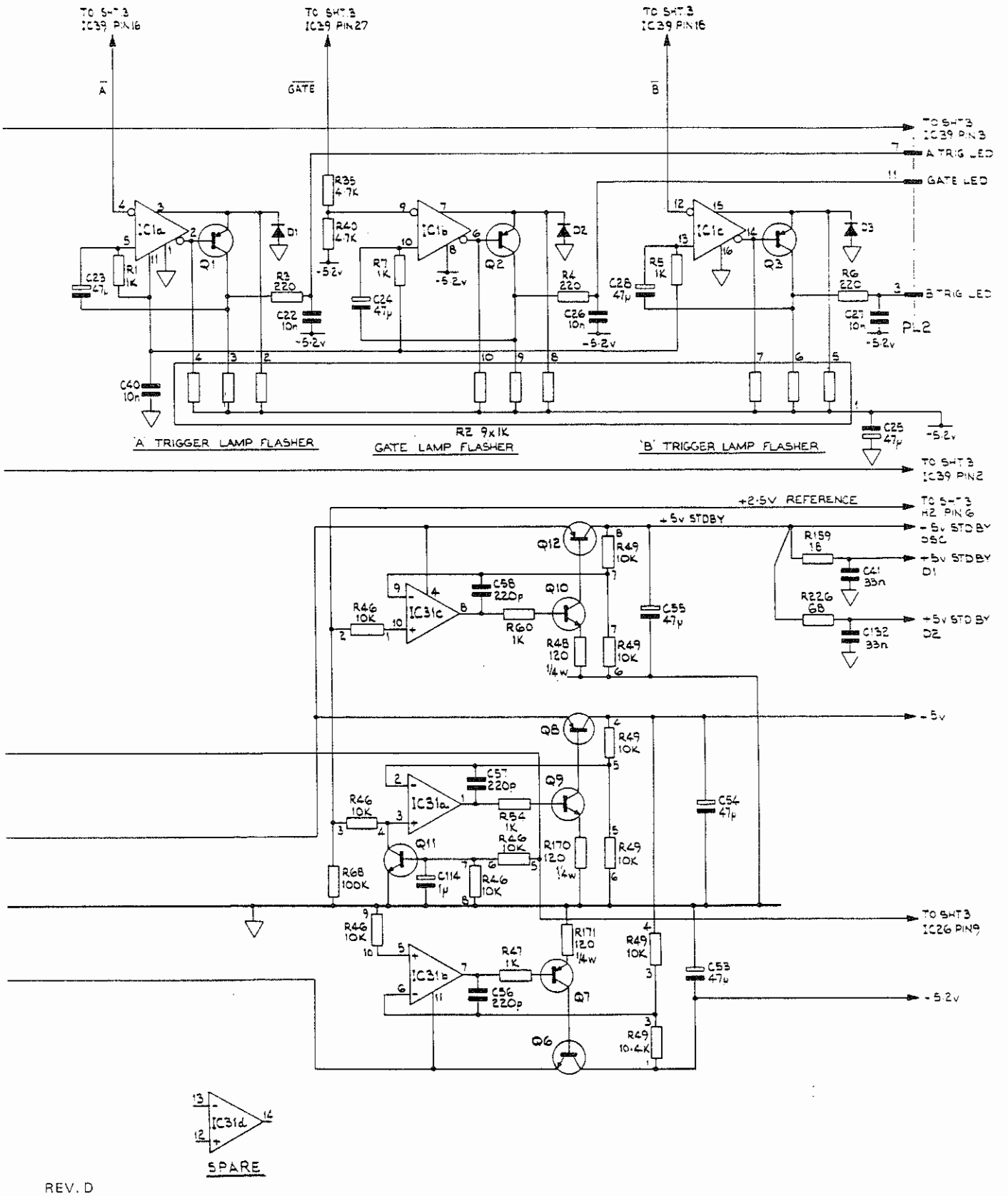
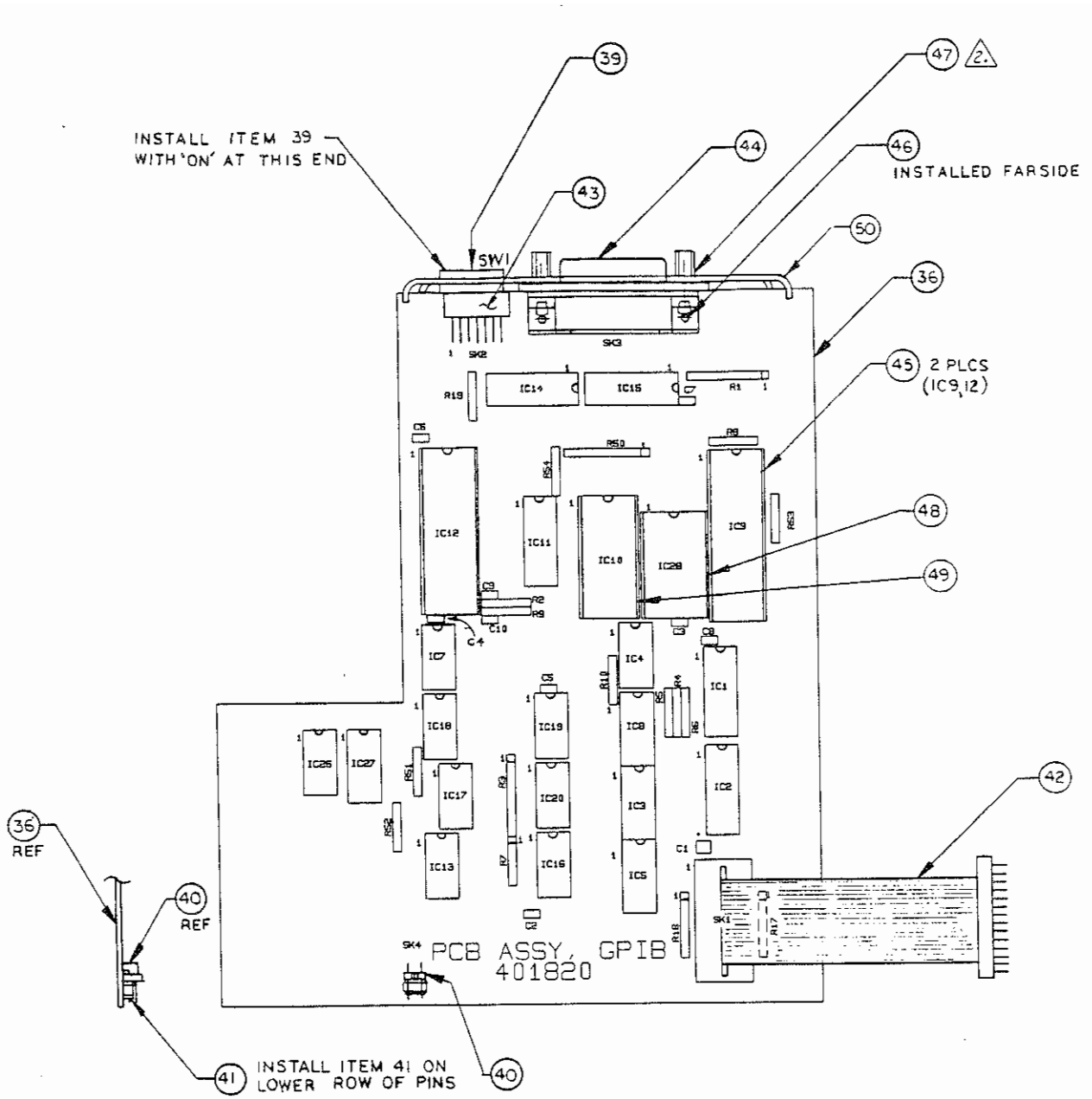


Figure 7.9 - Circuit Diagram, Motherboard (Cont'd)



2. DISCARD NUTS & LOCKWASHERS SUPPLIED WITH ITEM 47.

1. REF. SCHEM. 411820.

NOTES: UNLESS OTHERWISE SPECIFIED.

Figure 7.10 - Component Layout, GPIB (401820)

REV. A

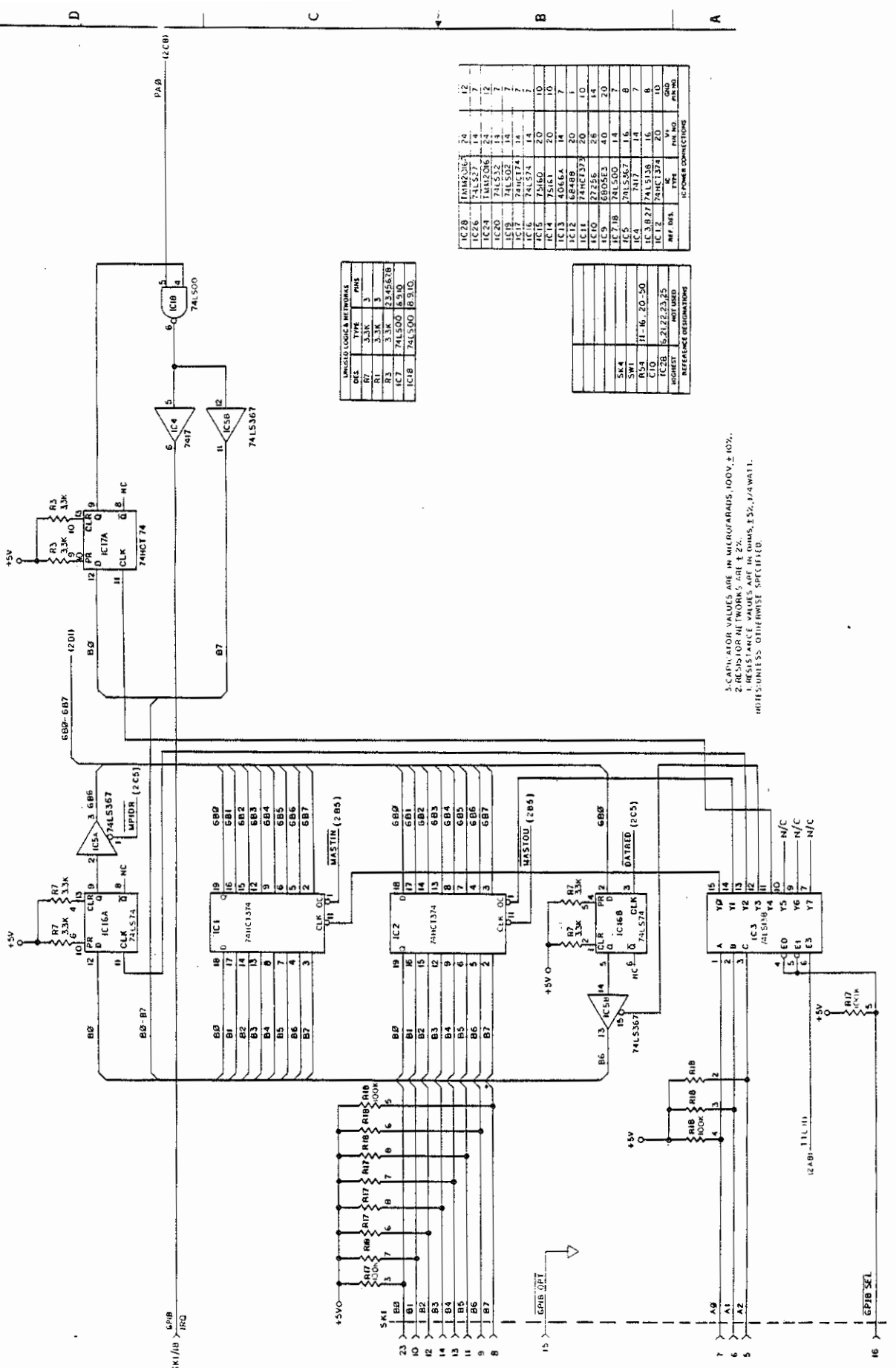


Figure 7.11 - Circuit Diagram, GPIB (431820)

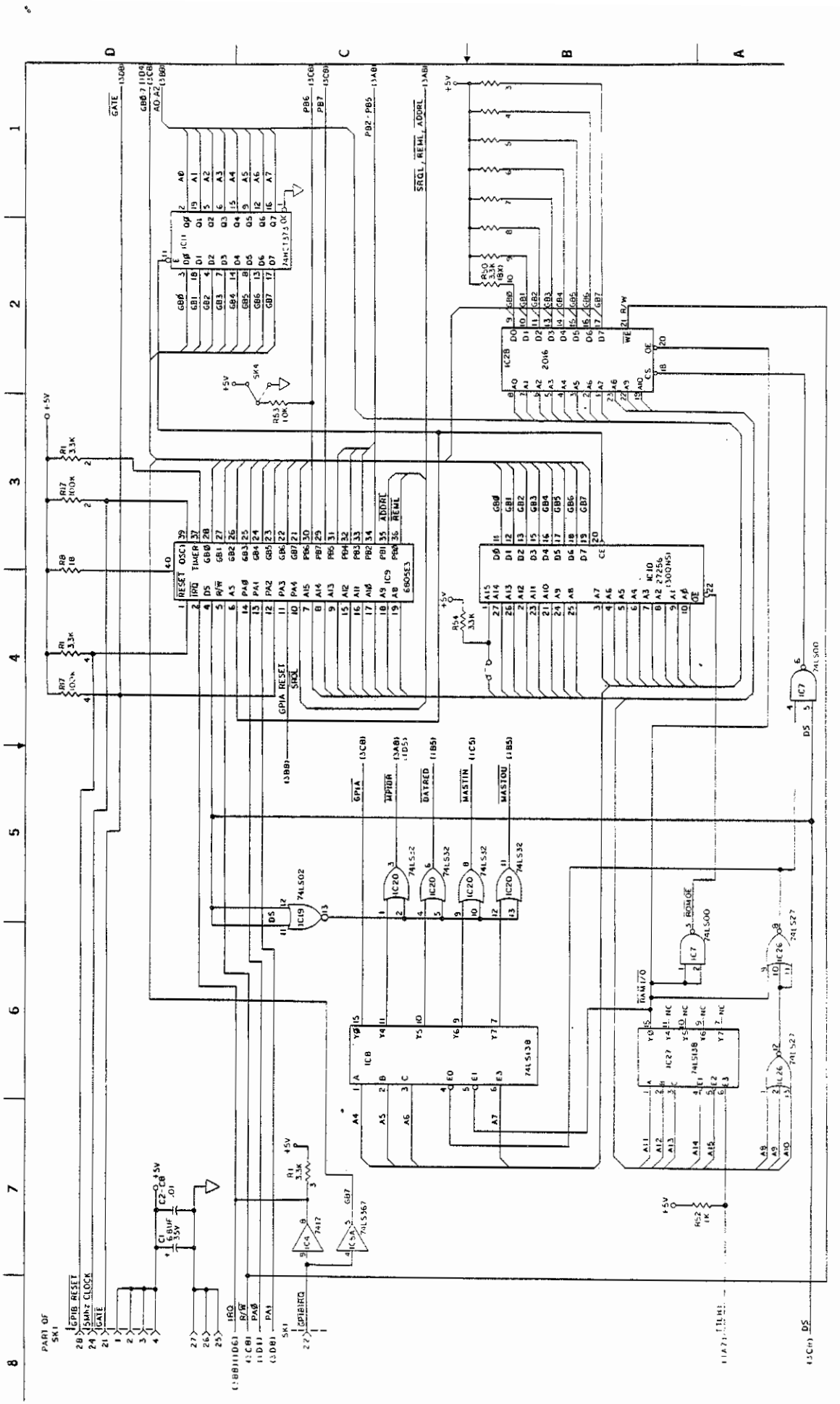


Figure 7.11 – Circuit Diagram, GPIB (431820) (Cont'd)

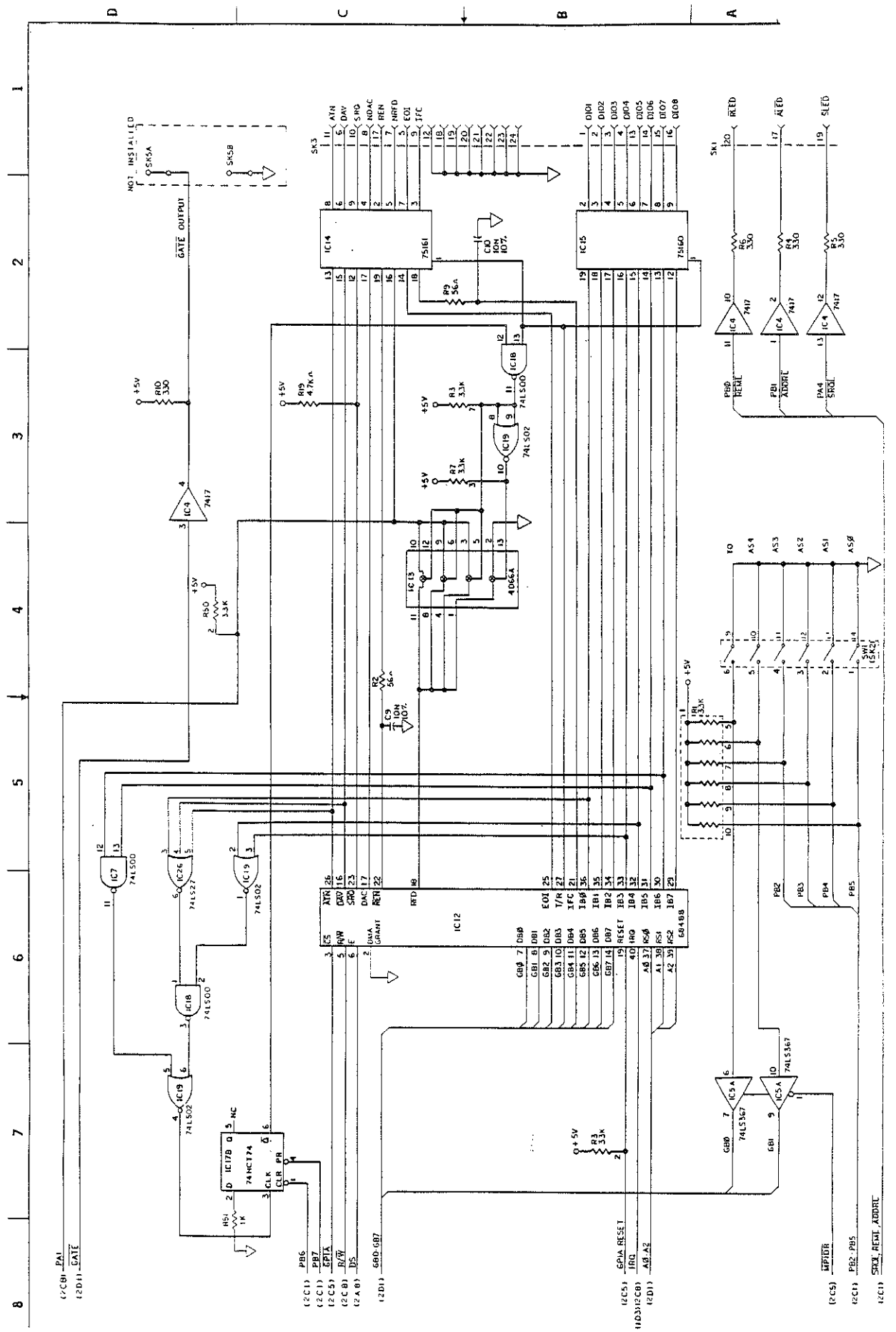
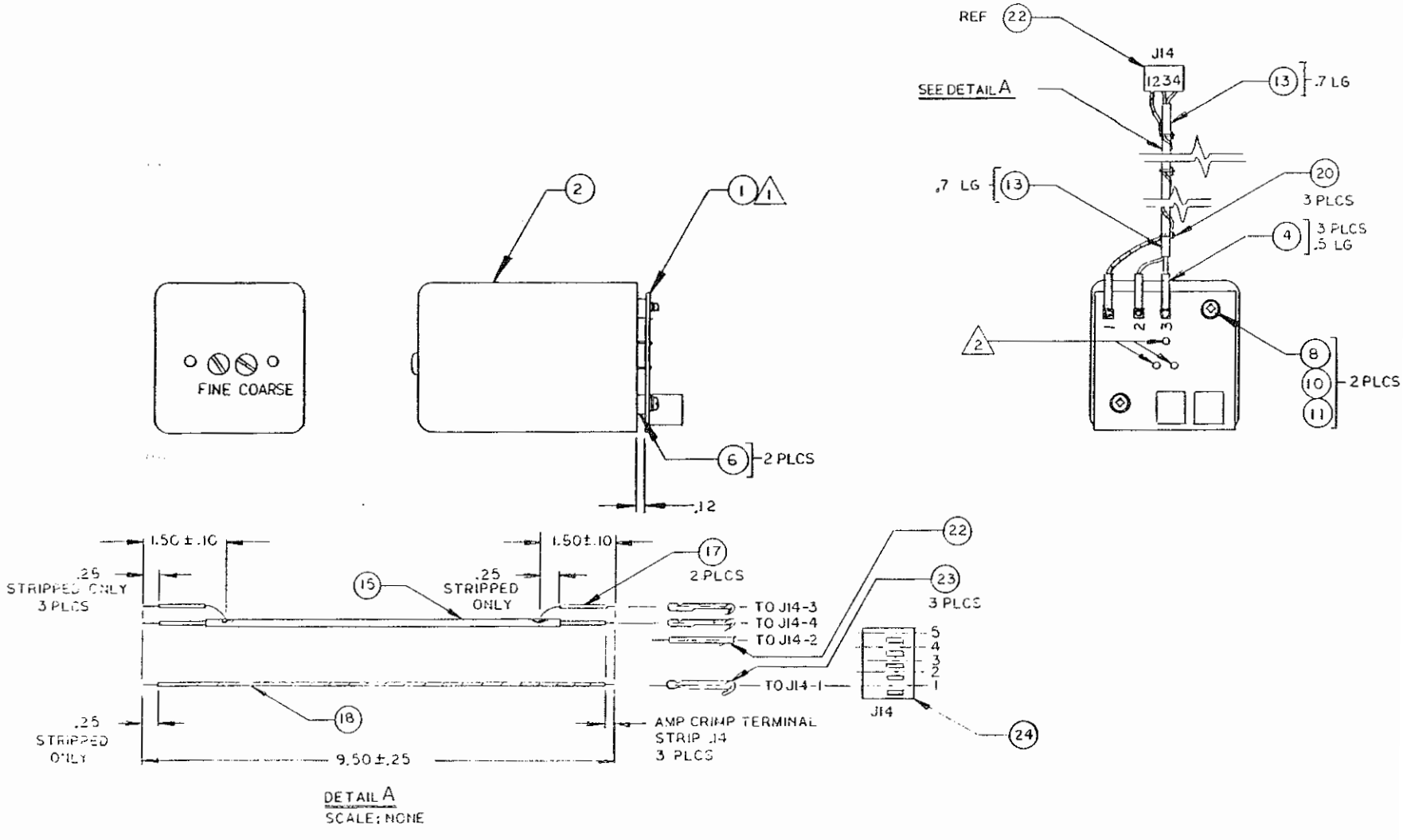


Figure 7.11 - Circuit Diagram, GPIB (431820) (Cont'd)

Figure 7.12 – Oscillator Assembly (404386)

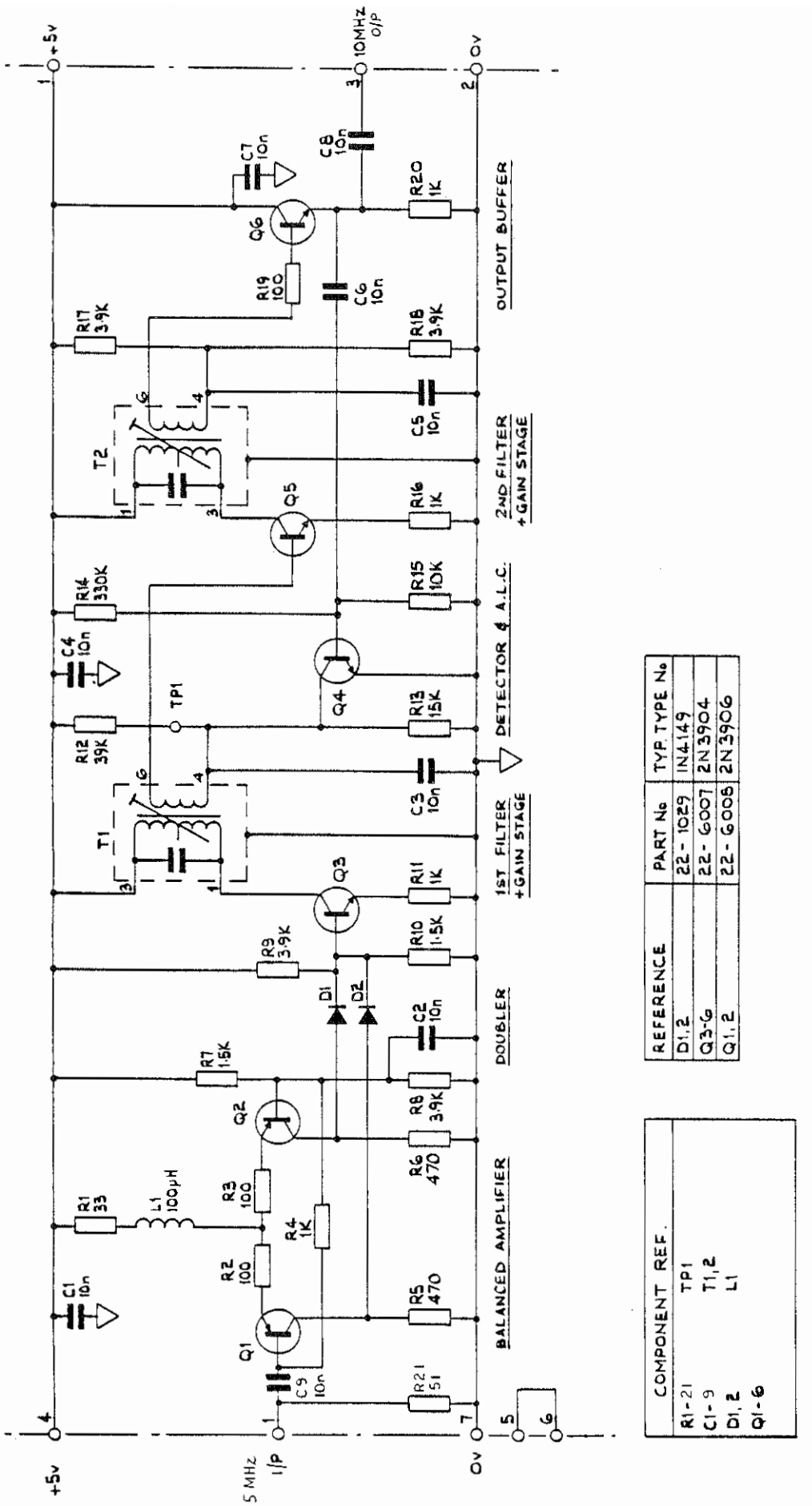


2. SOLDER AT ASSY.

1. REMOVE AND DISCARD CABLE SUPPLIED WITH ITEM 1 AND REPLACE WITH ITEMS: 4,13,15,17,18,20,22,23,24.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 7.13 - Component Layout, Doubler (401822)



7-26 **Figure 7.14 - Circuit Diagram, Doubler (431822)**

REV. A

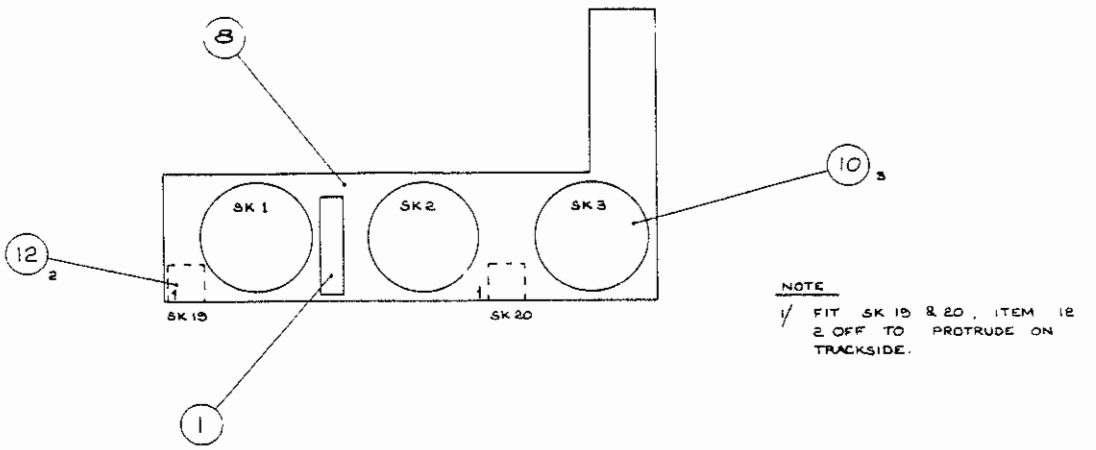


Figure 7.15 - Component Layout, BNC Mounting Board (19-1206)

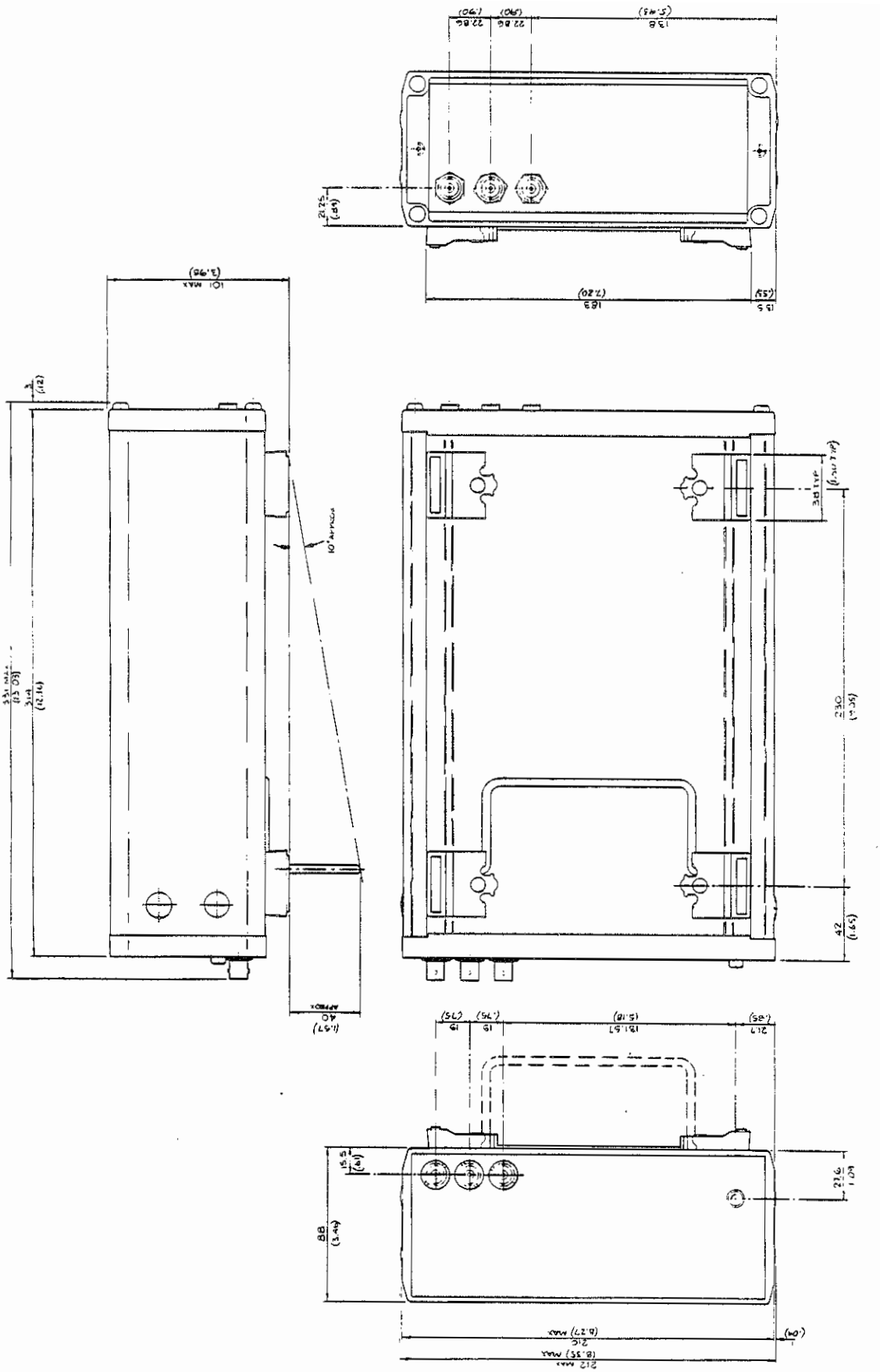


Figure 7.16 – Outline Drawing (455124)

SECTION 8 PARTS LIST

8.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

8.2 Manufacturers are identified by FSC numbers listed in Table 8.1, "List of Suppliers". The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbook H4-1, H4-2, and their supplements.

Table 8.1 - List of Suppliers

FSC	NAME
00779	AMP, INC. HARRISBURG, PA
01121	ALLEN BRADLEY CO. MILWAUKEE, WISCONSIN
01295	TEXAS INSTRUMENTS, INC. DALLAS, TEXAS
02114	FERROXCUBE CORP. SAUGERTIES, N.Y
02660	AMPHENOL CORP. BROADVIEW, ILLINOIS
04713	MOTOROLA, INC. (SEMI-CONDUCTOR PRODUCTS DIV.) PHOENIX, ARIZONA
05397	UNION CARBIDE CORP. (MATERIALS SYSTEMS DIV.) CLEVELAND, OHIO
05915	RICHCO PLASTIC CO. CHICAGO, ILLINOIS
07263	FAIRCHILD (SEMICONDUCTOR DIV.) MOUNTAIN VIEW, CA
11237	CTS KEENE, INC. PASO ROBLES, CA
13764	MICRO PLASTICS INC. FLIPPIN, AR
14433	ITT SEMICONDUCTORS WEST PALM BEACH, FLORIDA
14936	GENERAL INSTRUMENTS CORP. (SEMICONDUCTOR PRODUCTS GROUP) HICKSVILLE, L.I., N.Y.
16555	DENNISON MFG. CO. FRAMINGTON, MA
17856	SILICONIX, INC. SANTA CLARA, CA
18324	SIGNETICS CORP. SUNNYVALE, CA
18565	CHOMERICS, INC. WOBURN, MA
18714	RCA (COMMERCIAL REC. TUBE & SEMI. DIV.) FINDLAY, OH
19738	AVDEL-CHOBERT TELESBORO, NJ
1CJ86	BOSSARD BROOKFIELD, CT
21793	RACAL-DANA INSTRUMENTS INC. IRVINE, CA
22119	FERRANTI ELECTRIC PLAINVIEW, NY
22958	TELEDYNE ELECTRO MECHANISMS NASHUA, NH
24335	COOPER LABORATORIES, INC. WAYNE, NJ
24931	SPECIALTY CONNECTOR CO., INC. FRANKLIN, IN
24972	AEG-TELEFUNKEN CORP. SUMMERVILLE, NJ
25088	SIEMENS CORP. (COMP. GROUP) ISELIN, NJ
25403	AMPEREX ELECTRONIC CORP. (SEMICONDUCTOR & REC. TUBE DIV.) SLATERSVILLE, RHODE ISLAND
27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CA
27264	MOLEX PRODUCTS CO. DOWNERS GROVE, ILLINOIS
27777	VARO ELECTRAN DEVICES, INC. GARLAND, TX
28848	MULLARD, INC. FARMINGDALE, L.I., N.Y.
29005	STORM PRODUCTS CO. LOS ANGELES, CA
2V900	BULGIN A.F. AND CO., LTD. BARKING ESSEX, ENGLAND
32293	INTERSIL, INC. CUPERTINO, CA

Table 8.1 - List of Suppliers continued

FSC	NAME
32897	MURATA ERIE NORTH AMERICA INC. CARLISLE, PA
46384	PENN ENG. & MFG. CORP. DOYLESTOWN, PA
50434	HEWLETT-PACKARD CO. (HPA DIV.) PALO ALTO, CA
52072	CIRCUIT ASSY. CORP. COSTA MESA, CA
52210	KASON CORP. NEWARK, NJ
52648	PLESSEY MEMORIES SANTA ANA, CA
53387	THREE (3)M CO. (ELECTRONIC PRODUCTS DIV.) ST. PAUL, MN
56235	STATE OF THE ART INC. STATE COLLEGE, PA
57058	MATSUSHITA ELECTRIC CORP. OF AMERICA PANASONIC INDUSTRIAL CO. DIV. SECAUCUS, NJ
61802	TOSHIBA INTERNATIONAL HOUSTON, TX
61935	SCHURTER, INC. PETALUMA, CA
63878	AP PRODUCTS, INC. MENTOR, OH
65238	NOVACAP BURBANK, CA
65940	ROHM CORP. IRVINE, CA
70903	BELDEN CORP. CHICAGO, IL
71400	BUSSMAN MFG. (DIV. MCGRAW & EDISON CO.) ST. LOUIS, MO
71450	CTS CORP. ELKHART, IN
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PA

FSC	NAME
75915	LITTELFUSE, INC. DES PLAINES, IL
78189	ILLINOIS TOOL WORKS, INC. (SHAKEPROOF DIV.) ELGIN, IL
78553	EATON CORP. (TINNERMAN PRODUCTS, INC.) CLEVELAND, OH
80031	MEPCO-ELECTRA MORRISTOWN, NJ
81349	MILITARY SPECIFICATION
82219	PHILIPS ECG INC. DIV. OF NORTH AMERICAN PHILIPS CORP. EMPORIUM, PA
83125	NYTRONICS, INC. DARLINGTON, SC
83330	HERMAN H. SMITH, INC. BROOKLYN, NY
88044	AERONAUTICAL STANDARDS GROUP DEPT. OF NAVY AND AIR FORCE
8C945	ELECTRONIZED CHEMICAL CO. BALTIMORE, MD
91506	AUGAT, INC. ATTLEBORO, MA
91637	DALE ELECTRONICS, INC. COLUMBUS, NE
91718	GENTECH AN INDIAN HEAD CO. LINDEN, NJ
95275	VITRAMON, INC. BRIDGEPORT, CN
96906	MILITARY SPECIFICATION
K0536	HARWIN ENGINEERS HANTS, ENGLAND
K1160	WELWNY MICROELECTRONICS NORTHUMBERLAND, ENGLAND
K1935	JERMYN MANUFACTURING KENT, ENGLAND
K2324	WEBB FASTENERS BERKSHIRE, ENGLAND
U3065	TOKO BERKSHIRE, ENGLAND
U3441	QUADRANT METER CO., LTD. HERTS, ENGLAND

404503 - FINAL ASSY., 1992-02M, REV. B

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
{4}1	404506	CHASSIS ASSY.	21793	404506
{7}1	R-11-1650	COVER KIT ASSY.	21793	R-11-1650
{9}*	401820	PCB ASSY., GPIB	21793	401820
{12}*	R-13-1976	FRONT PANEL OVERLAY	21793	R-13-1976
{20}2	R-11-1728	BRACKET ASSY.	21793	R-11-1728
{22}2	R-24-0146	NUT, CAPTIVE "U" TYPE	21793	R-24-0146
{24}3	R-24-0245	BUTTON, RUBBER, GRAY, SELF-ADHESIVE	21793	R-24-0245
{25}2	617077	WASHER, INTERNAL LOCK, #4	88044	AN93A4C
{29}4	R-24-2816	WASHER, NYLON, #8	13764	113FW0008
{30}2	R-24-5835	SCREW, FL HD., #6 X .375, AB SELF-TAP	21793	R-24-5835
{31}1	980636	MANUAL, INSTRUCTION	21793	980636
{37}*	920756	FUSE, SLO-BLO, 250A, 250V	71400	MDL1/4
{38}4	R-24-7543	SCREW, CSK HD., M4 X 10	K2324	M4X10MMPOZI
{39}1	600620	CABLE, POWER, AC LINE	70903	172508
{40}2	616315	SCREW, PAN. HD., M3 X 6	1CJ86	7985-A-M3X6MM

404506, CHASSIS ASSEMBLY, REV. B

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
(4)1	R-11-1592	FRONT PANEL SUB ASSY.	21793	R-11-1592
(6)1	R-11-1593	REAR PANEL SUB. ASSY.	21793	R-11-1593
(8)1	455112	SHIELD, POWER	21793	455112
(14)2	R-11-1643	SIDE PANEL ASSY.	21793	R-11-1643
(20)1	R-13-2024	LID	21793	R-13-2024
(25)1	R-13-2102	KEEPER PLATE	21793	R-13-2102
(27)1	511072	SPACER, BNC	21793	R-14-1577
(32)1	R-15-0674	PUSH BUTTON MAINS	21793	R-15-0674
(34)1	R-15-0693	SWITCH CONTROL ROD	21793	R-15-0693
(36)1	455110	MAINS COVER	21793	455110
(42)1	R-17-1038	BNC-SMA FUSED SKT	03441	TG-5001
(48)1	R-18-1254	VOLTAGE SELECT BOARD	21793	R-18-1254
(50)1	R-18-1239	SCREEN	21793	R-18-1239
(52)1	R-19-1141	DISPLAY BOARD ASSY.	21793	R-19-1141
(54)1	R-19-1145	MOTHERBOARD ASSY.	21793	R-19-1145
(56)1	404386	OSCILLATOR ASSY., 5 MHZ	21793	404386
(58)1	R-19-1206	B.N.C. BOARD ASSY.	21793	R-19-1206
(62)1	R-19-1142	1.3 GHZ PRESCALER BD	21793	R-19-1142
(64)1	920204	FUSE, SLO-BLO, .50A, 250V	75915	323-500
(66)1	R-23-0053	FUSE HOLDER, CARRIER TOP	61935	FEK-031-1665
(70)1	R-24-0187	BUTTON, RUBBER	53387	SJ5023
(74,3	921065	CARD GUIDE, 3" LG	21793	921065
(76)1	R-24-0244	RIVET, PLASTIC, BLACK	06915	SR3045
(82)1	617042	NUT, HEX, M3	1CJ86	DIN934-M3
(84)1	617044	NUT, HEX, M4	1CJ86	DIN934-M4
(86)1	611153	NUT, TINNERMAN, TWIN TYPE, 4Z	78553	C6059-4Z-4
(92)16	R-24-2801	WASHER, CRINKLE, M3	21793	R-24-2801
(100)1	600191	LUG, SOLDER	83330	1416-8
(103)1	R-24-6127	LABEL, ALUMINUM	21793	R-24-6127
(108)9	616315	SCREW, PAN. HD., M3 X 5	1CJ86	7985-A-M3X6MM
(110)6	616316	SCREW, PAN. HD., M3 X 8	1CJ86	7985-A-M2.5X14MM
(112)2	611154	SCREW, PPH, 4B SELF TAP	21793	611154
(118)4	R-24-7822	SCREW, TAPTITE, M3 X 8	21793	R-24-7822
(125)20MM	500023	WIRE, BARE COPPER/TIN, 24 GA	21793	500023
(130)50MM	500215	WIRE, TEFLON STRANDED, 18 GA, GRN W/YEL	70903	83009-DARK
(136)35MM	R-25-5202	HEATSHRINK SLEEVING, .198 ID, BLK	21793	R-25-5202

R-19-1141, PCB ASSY., DISPLAY, REV. A

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1	100062	CAP, CER, .01 UF 100V, 10 PERCENT	05397	C320C103K1R5CA
C2	R-21-0785	CAP, ALUM. ELEC., 4.7 UF	61058	ECEA1HK4R7E
C3-5	100062	CAP, CER, .01 UF 100V, 10 PERCENT	05397	C320C103K1R5CA
D6-7	R-22-1029	DIODE, SILICON	14433	1N4149
D9-10	R-22-1029	DIODE, SILICON	14433	1N4149
DI1-4	R-26-1512	DISPLAY, DOUBLE DIGIT	14936	MAN6910
DI5	R-26-1513	DISPLAY, SINGLE DIGIT	14936	MAN6950
DI6	R-26-1511	DISPLAY, SINGLE DIGIT	25088	HDSP-5
IC1	R-22-4754	IC, DUAL 4-INPUT NAND GATES	18324	HEF4012BP
IC2	R-22-4779	IC, CMOS 16-KEY ENCODER	27014	MM74C922N/A
IC3-4	230457	IC, LED DRIVER	32293	ICM7218AIPI
LP1-8	R-26-5026	LED, RED	14936	MV6754-21
LP11-13	R-26-5026	LED, RED	14936	MV6754-21
LP15-18	R-26-5026	LED, RED	14936	MV6754-21
LP20-32	R-26-5026	LED, RED	14936	MV6754-21
LP33	R-26-5027	LED, ORANGE	24972	TLSO-360
LP34-42	R-26-5026	LED, RED	14936	MV6754-21
LP44-47	R-26-5026	LED, RED	14936	MV6754-21
R1-2	000103	RES, CARB COMP, 10K, 5 PERCENT 1/4W	21793	RC07GF103J
R3	080015	RES NETWORK, 9R, 10K, 5 PERCENT	71450	750-101-R10K
R4-5	000103	RES, CARB COMP, 10K, 5 PERCENT 1/4W	21793	RC07GF103J
S1-33	601211	SWITCH, PUSHBUTTON	U3065	R-7005
SK1-2	R-23-5160	SOCKET, 14-WAY	63878	929975-07
(2)21	R-15-0703	PUSH BUTTON, GREY	21793	R-15-0703
(4)4	R-15-0705	PUSH BUTTON, BLUE	21793	R-15-0705
(6)1	R-16-0651	BUTTON, PRINTED (NO. 1)	21793	R-16-0651
(7)1	R-16-0652	BUTTON, PRINTED (NO. 2)	21793	R-16-0652
(8)1	R-16-0653	BUTTON, PRINTED (NO. 3)	21793	R-16-0653
(9)1	R-16-0654	BUTTON, PRINTED (NO. 4)	21793	R-16-0654
(10)1	R-16-0655	BUTTON, PRINTED (NO. 5)	21793	R-16-0655
(11)2	R-16-0656	BUTTON, PRINTED (NO. 6 & 9)	21793	R-16-0656
(12)1	R-16-0657	BUTTON, PRINTED (NO. 7)	21793	R-16-0657
(13)1	R-16-0658	BUTTON, PRINTED (NO. 8)	21793	R-16-0658
(14)1	R-16-0659	BUTTON, PRINTED (NO. 0)	21793	R-16-0659
(15)1	R-16-0660	BUTTON, PRINTED (DECIMAL POINT)	21793	R-16-0660
(17)1	R-18-1141	P.C. BOARD (UNLOADED)	21793	R-18-1141
(58)1	920891	SOCKET, 28-PIN	52072	CA-28S-TSD-BC
(54)14	500002	TUBING, SHRINK, .187 ID	80945	M23053/5-105-0

R-19-1142, PCB ASSY., CHANNEL C, REV. B

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1-6	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C7	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C8-10	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C11	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C12-13	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C14	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C15	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C16	R-21-0795	CAP, ALUM. ELEC., 47 UF	28848	2222-036-35479
C17-18	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C19	R-21-1733	CAP, CHIP, 4.7 PF	95275	VJ1206N4R7CF
C21	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C22	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C23	R-21-1788	CAP, CHIP, 12 PF	95275	VJ1206A120JF
C24-25	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C26	R-21-1800	CAP, CHIP, 1 NF	95275	VJ1206Y102KF
C27	R-21-0795	CAP, ALUM. ELEC., 47 UF	28848	2222-036-35479
C28-32	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C33	R-21-1784	CAP, CHIP, 5.6 PF	95275	VJ1206A5R6CF
C34-36	R-21-1785	CAP, CHIP, 6.8 PF	95275	VJ1206A6R8CF
C37	R-21-1795	CAP, CHIP, 47 PG	95275	VJ1026A470JF
C38-39	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C40-41	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C42	R-21-1784	CAP, CHIP, 5.6 PF	95275	VJ1206A5R6CF
C43	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C44	R-21-0795	CAP, ALUM. ELEC., 47 UF	28848	2222-036-35479
C45	R-21-0704	CAP, ALUM. ELEC., 47 UF	28848	122-53479
C46	R-21-1782	CAP, CHIP, 3.9 PF	95275	VJ1206A3R9CF
C47-48	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C49-50	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C51-52	R-21-1789	CAP, CHIP, 15 PF	95275	VJ1026A150JF
C53	130133	CAP, CER, .1 UF, LOW PROFILE, 20 PERCENT	32897	8131LP-100-25U-104M
D1	210089	DIODE, LOW OFFSET SCHOTTKY	50434	HP5082-2835
D2	R-22-1058	DIODE, SILICON	50434	5082-3379
D3	210089	DIODE, LOW OFFSET SCHOTTKY	50434	HP5082-2835
D5-6	210089	DIODE, LOW OFFSET SCHOTTKY	50434	HP5082-2835
D7	R-22-1058	DIODE, SILICON	50434	5082-3379
D8-9	210017	DIODE, MATCHED PAIR	21793	210017
D10-11	R-22-1814	DIODE, ZENER	25403	BZX79C9V1
D12	R-22-1029	DIODE, SILICON	14433	1N4148
IC1	230547	IC, QUAD COMPARATOR	27014	LM339N/A-1
IC2	230787	IC, DIGITAL, TRIPLE LINE RECEIVER	04713	MC10116PDS
IC3	R-22-4594	IC, 1.3 GHZ PRESCALER	52648	SP4731
IC4	230193	IC, NAND GATE	01295	SN74LS00N3
L1	R-17-3240	COIL ASSY.	21793	R-17-3240
Q1-3	R-22-5123	TRANSISTOR, NPN	82219	BFR90
Q4	R-22-6155	TRANSISTOR, RF	50434	HXTR-3101
R3-4	R-20-5758	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R5	R-20-5841	RES, CHIP, 150 OHM, 1W	56235	2021CPX151J
R6	R-20-5837	RES, CHIP, 39 OHM, 1W	56235	2021CPX390J
R7	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R8	R-20-5783	RES, CHIP, 150 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-150 OHM-5 PCT
R9	R-20-5786	RES, CHIP, 270 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-270 OHM-5 PCT
R10	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT

R-19-1142, PCB ASSY., CHANNEL C, REV. B (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
R11	R-20-5786	RES, CHIP, 270 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-270 OHM-5 PCT
R12	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R13	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-33 OHM-5 PCT
R14	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R15	R-20-5786	RES, CHIP, 270 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-270 OHM-5 PCT
R16	R-20-5788	RES, CHIP, 390 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-390 OHM-5 PCT
R17	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R18	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-33 OHM-5 PCT
R20	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R21-22	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-180 OHM-5 PCT
R23	R-20-5788	RES, CHIP, 390 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-390 OHM-5 PCT
R24	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R25	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-33 OHM-5 PCT
R26	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R27	R-20-7049	POT, 20K PRE-SET	21793	R-20-7049
R28	R-20-5788	RES, CHIP, 390 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-390 OHM-5 PCT
R29	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PERCENT, 200V	65940	MCR18-100K-5 PCT
R30	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R31	R-20-5774	RES, CHIP, 22 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-22 OHM-5 PCT
R32	R-20-5785	RES, CHIP, 220 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-220 OHM-5 PCT
R33-34	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1.5K-5 PCT
R35	R-20-5810	RES, CHIP, 56K, 1/8W, 5 PERCENT, 200V	65940	MCR18-56K OHM-5 PCT
R36	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R37	R-20-5779	RES, CHIP, 56 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-56 OHM-5 PCT
R38	R-20-5810	RES, CHIP, 56K, 1/8W, 5 PERCENT, 200V	65940	MCR18-56K OHM-5 PCT
R39	R-20-5770	RES, CHIP, 1M, 1/8W, 5 PERCENT	65940	1M OHM-5 PCT
R41-42	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5 PERCENT, 200V	65940	MCR18-4.7K-5 PCT
R44	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R45	R-20-5783	RES, CHIP, 150 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-150 OHM-5 PCT
R46-49	R-20-5775	RES, CHIP, 27 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-27 OHM-5 PCT
R50	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R52	R-20-5801	RES, CHIP, 6.8K, 1/8W, 5 PERCENT, 200V	65940	MCR18-6.8K-5 PCT
R53	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.3K-5 PCT
R54-55	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R56	R-20-5790	RES, CHIP, 680 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-680 OHM-5 PCT
R57	R-20-5766	RES, CHIP, 2.7K, 1/8W, 5 PERCENT	65940	MCR18-2.7K OHM-5 PCT
R58	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.3K-5 PCT
R59-62	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R65	R-20-5783	RES, CHIP, 150 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-150 OHM-5 PCT
R68-69	R-20-5770	RES, CHIP, 1M, 1/8W, 5 PERCENT	65940	1M OHM-5 PCT
R70-71	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
SK7	R-23-5173	CONNECTOR, 30-WAY	K0536	M20-989-30-06
(4)1	R-10-2891	COAX ASSY.	21793	R-10-2891
(5)1	R-11-1737	COVER ASSY.	21793	R-11-1737
(6)2	R-13-2103	SCREEN	21793	R-13-2103
(7)1	R-13-2104	COVER	21793	R-13-2104
(8)2	R-14-4000	SPACER	21793	R-14-4000
(10)1	R-18-1142	P.C. BOARD (UNLOADED)	21793	R-18-1142
(156)2	617042	NUT, HEX, M3	1CJ86	DIN934-M3
(158)2	R-24-2801	WASHER, CRINKLE, M3	21793	R-24-2801
(166)60MM	500022	WIRE, BARE COPPER/TIN, 22 GA	21793	500022

R-19-1145, PCB ASSY., MOTHERBOARD, REV. D

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C2	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C3	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C4-12	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C13-14	R-21-1800	CAP, CHIP, 1 NF	95275	VJ1206Y102KF
C22	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C23-25	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C26-27	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C28	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C35	R-21-1800	CAP, CHIP, 1 NF	95275	VJ1206Y102KF
C36	R-21-1847	CAP, CHIP, 20 NF, 400V	65238	1206B203K401N
C37	R-21-1809	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C40	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C41-45	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C46	R-21-7003	CAP, POLYPROP., 47 NF, 250V	25088	CB1121-C-123
C47-48	R-21-7002	CAP, POLYPROP., 2.5 NF	25088	CB1121-C-B141
C49	R-21-0583	CAP, ALUM. ELEC., 10000 UF, 16V	28848	2222-050-55103
C50	R-21-0567	CAP, ALUM. ELEC., 4700 UF, 16V	28848	2222-050-55472
C52	R-21-0797	CAP, ALUM. ELEC., 680 UF, 25V	28848	2222-035-56681
C53-55	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C56-58	R-21-1838	CAP, CHIP, 220 PF	95275	VJ1206A221JF
C59	R-21-0797	CAP, ALUM. ELEC., 680 UF, 25V	28848	2222-035-56681
C65-66	R-21-1847	CAP, CHIP, 20 NF, 400V	65238	1206B203K401N
C67	R-21-1859	CAP, CHIP, 6.8 PF, 400V	95275	VJ1206A6RBCX7400
C68	R-21-1862	CAP, CHIP, 47 PF, 2 PCT	95275	VJ1206A470GXA
C69	R-21-1859	CAP, CHIP, 6.8 PF, 400V	95275	VJ1206A6RBCX7400
C70	R-21-1862	CAP, CHIP, 47 PF, 2 PCT	95275	VJ1206A470GXA
C71	R-21-1780	CAP, CHIP, 2.7 PF	95275	VJ1206A2R7CF
C72	R-21-1782	CAP, CHIP, 3.9 PF	95275	VJ1206A3R9CF
C73-74	R-21-1857	CAP, CHIP, 100 PF, 400V	65238	1206N101K401N
C75-78	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C79	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C80	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y104MF
C81	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C82	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C83	100133	CAP, CER, .1 UF, LOW PROFILE, 20 PERCENT	32897	8131LP-100-25U-104M
C84-85	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C86	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C87	R-21-1858	CAP, CHIP, 3.3 NF, 50V	95275	VJ1206Y332KF
C88	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C89	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C90-91	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C92	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C93	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C94-95	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C96-103	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C104-105	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C106	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C107-108	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C109-110	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C111-113	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C114	R-21-0779	CAP, ELECT, 1 UF, 50V	61058	ECEA1HKP1PE
C115	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF

R-19-1145, PCB ASSY., MOTHERBOARD, REV. D (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C116	R-21-0739	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C117	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C118	R-21-1800	CAP, CHIP, 1 NF	95275	VJ1206Y102KF
C119	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C120	R-21-0739	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C121	R-21-0779	CAP, ELECT, 1 UF, 50V	61058	ECEA1HKP1R0E
C125	R-21-0739	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C126	R-21-0779	CAP, ELECT, 1 UF, 50V	61058	ECEA1HKP1R0E
C127	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C128	R-21-1800	CAP, CHIP, 1 NF	95275	VJ1206Y102KF
C129	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C130-131	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C132	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C133	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C225-226	R-21-0739	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
D1-4	R-22-1029	DIODE, SILICON	14433	1N4149
D5	R-22-1099	DIODE, SILICON	17856	JPAD50
D6-7	R-22-1029	DIODE, SILICON	14433	1N4149
D8	R-22-1099	DIODE, SILICON	17856	JPAD50
D11	R-22-1662	DIODE, BRIDGE RECTIFIER	27777	VH248
D12	R-22-1554	DIODE, BRIDGE, 800 DF	27777	VM18
D13-15	R-22-1029	DIODE, SILICON	14433	1N4149
D18-25	210099	DIODE, LOW OFFSET SCHOTTKY	50434	HP5082-2835
D26	R-22-1029	DIODE, SILICON	14433	1N4149
D28	R-22-1029	DIODE, SILICON	14433	1N4149
D30-31	R-22-1801	DIODE, VOLTAGE REGULATOR, 2.7V, 400 MW	14433	ZPD2.7
D32-33	R-22-1809	DIODE, VOLTAGE REGULATOR, 5.6V, 400 MW	14433	ZF.5.6A
FB1	R-23-0062	FUSE HOLDER	61935	FAU-031-3573
H1	R-17-1034	HYBRID TEC	21793	R-17-1034
H2	R-17-1035	HYBRID DAC	21793	R-17-1035
IC1	230750	IC, DIGITAL, ECL	04713	MC10216PDS
IC2	230787	IC, DIGITAL, TRIPLE LINE RECEIVER	04713	MC10116PDS
IC3	230200	IC, 12 VDC REGULATOR	04713	MC7812CT
IC4	230201	IC, REGULATOR	07263	UA7912UCQR
IC14	230787	IC, DIGITAL, TRIPLE LINE RECEIVER	04713	MC10116PDS
IC18	230790	IC, DIGITAL, CUSTOM CHIP	21793	230790
IC19	R-22-8307	IC, 8-BIT CMOS MICROPROCESSOR	04713	MC146805E2P
IC20	230805	IC, OCTAL TRANSPARENT LATCH, 3-STATE OUTPUT	18714	CD74HCT373EX
IC21	230358	IC, DEMULTIPLEXER	27014	SN74LS139N3
IC22	230367	IC, MEMORY	21793	230967
IC23	R-22-4807	IC, OCTAL BUFFER/LINE DRIVER, 3-STATE	18714	CD74HCT244E
IC24	230551	IC, OCTAL LATCH	18324	N74LS367N-B
IC25	230805	IC, OCTAL TRANSPARENT LATCH, 3-STATE OUTPUT	18714	CD74HCT373EX
IC26	230194	IC, DUAL D FLIP-FLOP	01295	SN74LS74AN3
IC27	230428	IC, QUAD 2 INPUT OR GATE	01295	SN74LS32N3
IC28	230248	IC, POSITIVE NAND GATE	01295	SN74LS1CN3
IC29	230234	IC, HEX INVERTER	01295	SN74LS04N
IC30	R-22-4700	IC, QUAD 2-INPUT NAND GATE	21793	R-22-4700
IC31	R-22-4262	IC, QUAD OP-AMP	07263	UA3403PC
IC32	R-22-4756	IC, HEX SCHMITT TRIGGER	18324	HEF40106BP
IC34-35	R-22-4269	IC, MOS/FET INPUT, BI POLAR OUTPUT OP-AMP	18714	CA3140E
IC36	230735	IC, COMPARATOR, DUAL ULTRA FAST	51870	AD9687BD
IC39	230789	IC, DIGITAL, CUSTOM CHIP	21793	230789

R-19-1145, PCB ASSY., MOTHERBOARD, REV. D (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
IC41	230733	IC, DIGITAL, ECL FLIP-FLOP	04713	MC10231PDS
L1-2	R-23-7217	CHOKE, MAINS, 40 UH	25088	BB22111-A-C7
L5-11	310151	CHOKE, 10 PERCENT, 100 UH	83125	DD100UH
L14-15	310152	CHOKE, WIDEBAND	02114	VK200-10/3B
L20	310151	CHOKE, 10 PERCENT, 100 UH	83125	DD100UH
LK1	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	530153-2
LK2-3	600245	JUMPER, INSULATED	52210	L-2007-1
LK4	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	530153-2
PL1-2	601250	CONN, 14-PIN RT. ANGLE, DUAL ROW	52072	CA-D14R-23B-43
PL7	601208-013	CONN., PCB, PLUG, 30-PIN	52072	CA-S30-23B-43
PL14	601208-012	CONN, PCB, PLUG, 5-PIN	52072	CA-S05-23B-43
PL15	601208-016	CONN, PCB, PLUG, 3-PIN	52072	CA-S03-23B-43
PL16	601208-015	CONN., PCB, PLUG, 10-PIN	52072	CA-S10-23B-43
PL17	601208-012	CONN, PCB, PLUG, 5-PIN	52072	CA-S05-23B-43
PL19	R-23-5176	PLUG, 2 X 3-WAY	27264	10-90-1061
PL20	R-23-5161	PLUG, RT. ANGLE, 2 ROW, 2 PIN	63878	929838-01-02
PL21	R-23-5168	PLUG, 2 X 10, 10-WAY	K0536	M20-998-10-06
Q1-3	R-22-6018	TRANSISTOR, PNP	04713	MPS3640
Q4	200299	TRANS, NPN	04713	2N3904
Q5	200299	TRANS, NPN	04713	2N3904
Q6	200302	TRANSISTOR, NPN	04713	MJE3055T
Q7	R-22-6113	TRANSISTOR, PNP	22119	ZTX550
Q8	200301	TRANSISTOR, PNP	04713	MJE2955T
Q9	R-22-6112	TRANSISTOR, NPN	22119	ZTX450
Q10	R-22-6112	TRANSISTOR, NPN	22119	ZTX450
Q11	200298	TRANS, NPN	04713	2N3904
Q12	200301	TRANSISTOR, PNP	04713	MJE2955T
Q13	R-22-6113	TRANSISTOR, PNP	22119	ZTX550
Q14	200298	TRANS, NPN	04713	2N3904
Q15-16	R-22-6163	TRANSISTOR, N-CH SILICON JFET	28848	BF256A
Q17-18	R-22-6206	TRANSISTOR, RF, NPN	22119	BFS17
Q21	R-22-6206	TRANSISTOR, RF, NPN	22119	BFS17
Q22	200298	TRANS, NPN	04713	2N3904
Q23	R-22-6206	TRANSISTOR, RF, NPN	22119	BFS17
Q24	200298	TRANS, NPN	04713	2N3904
Q25-27	200299	TRANS, PNP	04713	2N3906
Q28	R-22-6113	TRANSISTOR, PNP	22119	ZTX550
Q29	R-22-4216	IC, LINEAR HIGH CURRENT	18714	CA3083E
R1	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R2	R-20-5541	RES ARRAY, 9 X 1K OHM, 10 PIN SIL	81349	710A1C2
R3-4	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R5	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R6	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R7	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R8	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R11	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R16	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R18	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R25	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R28	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R32	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R33	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R35	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5 PERCENT, 200V	65940	MCR18-4.7K-5 PCT

R-19-1145, PCB ASSY., MOTHERBOARD, REV. D (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
R40	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5 PERCENT, 200V	65940	MCR18-4.7K-5 PCT
R45	000391	RES, CARBON, 390 OHM 1/4W, 5 PERCENT	81349	RC07GF390J
R46	R-20-5562	RES ARRAY, 10K, 10 PIN	61058	EXBF10V103G
R47	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R48	000121	RES, CARBON, 120 OHM, 1/4W, 5 PERCENT	81349	RC07GF120J
R49	R-20-5556	CUSTOM RES ARRAY, SIL	K1160	747026
R54	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R60	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R63	000391	RES, CARBON, 390 OHM 1/4W, 5 PERCENT	81349	RC07GF390J
R65	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R67	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R68	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PERCENT, 200V	65940	MCR18-100K-5 PCT
R75	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R76	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PERCENT, 200V	65940	MCR18-100K-5 PCT
R77	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R78-81	001875	RES, CARBON, 100 OHM, 1/2W, 5 PERCENT	01121	RC20GF101J
R82	010990	RES, CARBON FILM, 900K, 1/2W, 0.25 PERCENT	80031	RN55C9003B
R83	010989	RES, METAL FILM, 111K, 1/8W, 0.25 PERCENT	80031	RN55C1113B
R84	010990	RES, CARBON FILM, 900K, 1/2W, 0.25 PERCENT	80031	RN55C9003B
R85	010989	RES, METAL FILM, 111K, 1/8W, 0.25 PERCENT	80031	RN55C1113B
R87-89	R-20-5554	CUSTOM RES ARRAY, SIL	21793	R-20-5554
R91	R-20-5554	CUSTOM RES ARRAY, SIL	21793	R-20-5554
R93	R-20-5817	RES, CHIP, 560K, 1/8W, 5 PERCENT, 200V	65940	MCR18-560K-5 PCT
R94	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-180 OHM-5 PCT
R95	R-20-5817	RES, CHIP, 560K, 1/8W, 5 PERCENT, 200V	65940	MCR18-560K-5 PCT
R96	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-180 OHM-5 PCT
R97	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R98	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R100	R-20-5793	RES, CHIP, 1.2K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1.2K-5 PCT
R101	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R102	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R104	R-20-5793	RES, CHIP, 1.2K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1.2K-5 PCT
R107	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R110	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R111-112	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R113	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R115	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R116	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R117	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R119	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R120	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R121-124	R-20-5796	RES, CHIP, 2.2K, 1/8W, 5 PERCENT, 200V	65940	MCR18-2.2K-5 PCT
R125-126	R-20-5790	RES, CHIP, 680 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-680 OHM-5 PCT
R128	R-20-5785	RES, CHIP, 220 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-220 OHM-5 PCT
R129	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1.5K-5 PCT
R135	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PERCENT, 200V	65940	MCR18-100K-5 PCT
R136	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R137	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R139	000100	RES, CARBON, 10 OHM, 1/4W, 5 PERCENT	81349	RC07GF100J
R140	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R141	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R142	R-20-5780	RES, CHIP, 68 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-68 OHM-5 PCT
R143	000100	RES, CARBON, 10 OHM, 1/4W, 5 PERCENT	81349	RC07GF100J
R144	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT

R-19-1145, PCB ASSY., MOTHERBOARD, REV. D (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
R145	R-20-5758	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R146	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R147	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R148	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.3K-5 PCT
R149-150	R-20-7071	POT, 10K, TOP ADJ	21793	R-20-7071
R151-152	R-20-5758	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R155-156	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5 PERCENT, 200V	65940	MCR18-4.7K-5 PCT
R157	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PERCENT, 200V	65940	MCR18-100K-5 PCT
R158	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5 PERCENT, 200V	65940	MCR18-4.7K-5 PCT
R159	R-20-5763	RES, CHIP, 18 OHM, 1/8W, 5 PERCENT	65940	MCR18-18 OHM-5 PCT
R160	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R161	R-20-5780	RES, CHIP, 68 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-68 OHM-5 PCT
R163	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R164	R-20-5780	RES, CHIP, 68 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-68 OHM-5 PCT
R165-166	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R167-168	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.3K-5 PCT
R169	R-20-5778	RES, CHIP, 47 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-47 OHM-5 PCT
R170-171	000121	RES, CARBON, 120 OHM, 1/4W, 5 PERCENT	81349	RC07GF120J
R174	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R175	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R177	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R178	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.3K-5 PCT
R179	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R180	R-20-5758	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R181	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R186-187	R-20-5817	RES, CHIP, 560K, 1/8W, 5 PERCENT, 200V	65940	MCR18-560K-5 PCT
R188	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R189	R-20-5806	RES, CHIP, 27K, 1/8W, 5 PERCENT, 200V	65940	MCR18-27K-5 PCT
R190	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R191	R-20-5806	RES, CHIP, 27K, 1/8W, 5 PERCENT, 200V	65940	MCR18-27K-5 PCT
R192-193	R-20-7071	POT, 10K, TOP ADJ	21793	R-20-7071
R194	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R195	R-20-5774	RES, CHIP, 22 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-22 OHM-5 PCT
R196	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-180 OHM-5 PCT
R198	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R199	R-20-5774	RES, CHIP, 22 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-22 OHM-5 PCT
R200	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-180 OHM-5 PCT
R202-203	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R204	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5 PERCENT, 200V	65940	MCR18-4.7K-5 PCT
R205-210	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R211-213	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R214	R-20-5796	RES, CHIP, 2.2K, 1/8W, 5 PERCENT, 200V	65940	MCR18-2.2K-5 PCT
R215	R-20-5758	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R216	R-20-5780	RES, CHIP, 68 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-68 OHM-5 PCT
R217	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PERCENT, 200V	65940	MCR18-100K-5 PCT
R218-225	R-20-5758	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R226	R-20-5780	RES, CHIP, 68 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-68 OHM-5 PCT
R227	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R228	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R229	R-20-5796	RES, CHIP, 2.2K, 1/8W, 5 PERCENT, 200V	65940	MCR18-2.2K-5 PCT
RLA-RLD	R-23-7529	RELAY, REED, 1A	91718	G57DX424
RLE	R-23-7530	RELAY, DIL, 1 FORM C	91718	GT831C-238
RLF-RLG	R-23-7528	RELAY, REED, 1A18	21793	R-23-7528
RLH	R-23-7527	RELAY, DPDT	22958	172-5

R-19-1145, PCB ASSY., MOTHERBOARD, REV. D (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
S1	R-23-4124	MAINS SWITCH	21793	R-23-4124
SK5-6	501234	CONNECTOR, BNC, PCB MOUNT	U3441	TG-5000
SK8	R-23-5177	MAINS SELECTOR SOCKET	27264	09-03-1061
SK10	R-23-3429	MAINS SOCKET	2V900	9580/PC
T1	R-17-4102	TRANSFORMER, MAINS	21793	R-17-4102
(2)*	455117	HEATSINK ASSY.	21793	455117
(3)*	R-11-1706	CLAMP ASSY.	21793	R-11-1706
(4)*	R-13-1988	SCREEN	21793	R-13-1988
(5)*	R-13-2038	INSULATOR	21793	R-13-2038
(18)*	R-18-1145	P.C. BOARD, MOTHERBOARD (UNLOADED)	21793	R-18-1145
(381)3	611059	CONN, DIP, LOW PROFILE, 40-PIN	91506	240-AG39D
(386)2	920891	SOCKET, 28-PIN	52072	CA-28S-TSO-BC
(437)2	R-23-9148	INSULATING BUSH, M3	K1935	J22-5006
(439)5	610351	INSULATOR, TO-220	18565	6C-11-5791-1674
(442)4	617041	NUT, HEX, M2.5	1CJ86	DIN934-M2.5
(444)4	617042	NUT, HEX, M3	1CJ86	DIN934-M3
(446)4	R-24-2800	WASHER, M2,5	21793	R-24-2800
(447)6	R-24-2801	WASHER, CRINKLE, M3	21793	R-24-2801
(448)1	R-24-2802	WASHER, M4	21793	R-24-2802
(449)3	R-24-2805	WASHER, M3.5	21793	R-24-2805
(450)12	R-24-3519	AV LUGS	19738	AVLUG1107/020B
(452)1	R-24-4146	STAND-OFF, M3 X 14	46384	KTF-M3-14-ET
(454)4	616306	SCREW, PAN. HD., M2.5 X 14	21793	616306
(455)5	616316	SCREW, PAN. HD., M3 X 8	1CJ86	7985-A-M2.5X14MM
(459)*	615344	SCREW, PAN HD., M4 X 12	1CJ86	7985-A-M4X12MM
(460)3	616328	SCREW, PAN HD., M3.5 X 6	1CJ86	7985-A-M3.5X6MM
(468)70MM	520999	WIRE, TEFLON STRANDED, 20 GA, WHITE	21793	520999
(470)70MM	520909	WIRE, TEFLON STRANDED, 20 GA, WHT/BK	92194	5856/7 WHT/BLK
(472)70MM	520929	WIRE, TEFLON STRANDED, 20 GA, WHT/RED	21793	520929
(475)40MM	500009	TUBING, SHRINK, .125 ID, BLK	29005	RNF-100-1-1/8

401820, PCB ASSY., GPIB, REV. A

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1	110110	CAP, TANTA, 6.8 UF, 20V, 10 PERCENT	05397	T350B115K020AS
C2-10	100052	CAP, CER, .01 UF 100V, 10 PERCENT	05397	C320C103K1R5CA
IC1-2	230302	IC, OCTAL D-TYPE F-F, 3-STATE	18714	CD74HCT374EX
IC3	230368	IC, DEMULTIPLEXER	27014	SN74LS138N3
IC4	230105	IC, HEX BUFFER/DRIVER	01295	SN7417N3
IC5	230330	IC, TRI-STATE BUFFER	01295	SN74LS367AN3
IC7	230193	IC, NAND GATE	01295	SN74LS00N3
IC8	230368	IC, DEMULTIPLEXER	27014	SN74LS138N3
IC9	230821	IC, CPU, CMOS, 64K EXT MEMORY	18714	CD6805E33X
IC10	230917	IC, MEMORY	21793	230917
IC11	230305	IC, OCTAL TRANSPARENT LATCH, 3-STATE OUTPUT	18714	CD74HCT373EX
IC12	230430	IC, GENERAL PURPOSE INTERFACE ADAPTER	04713	MC68488P
IC13	230247	IC, MOS BILATERAL SWITCH	18714	CD4066AEX
IC14	230472	IC, OCTAL GPIB TRANS	01295	SN75161AN3
IC15	230459	IC, OCTAL GPIB TRANS	01295	SN75160AN3
IC16	230194	IC, DUAL D FLIP-FLOP	01295	SN74LS74AN3
IC17	230798	IC, QUAD D W/SET & RESET	18714	CD74HCT74EX
IC18	230193	IC, NAND GATE	01295	SN74LS00N3
IC19	230306	IC, QUAD, 2 INPUT NOR GATES	01295	SN74LS02N3
IC20	230428	IC, QUAD 2 INPUT OR GATE	01295	SN74LS32N3
IC26	230715	IC, DIGITAL, 3 INPUT NOR	01295	SN74LS27N3
IC27	230368	IC, DEMULTIPLEXER	27014	SN74LS138N3
IC28	230648	IC, MEMORY, 2K X 8 RAM	61802	TMM2016P
R1	080082	RES NETWORK, 10P, 9RES, 3.3K, 2 PERCENT	11237	750-101-R3.3K
R2	000560	RES, CARB COMP, 56 OHM, 5 PERCENT 1/4W	81349	RC07GF560J
R3	080082	RES NETWORK, 10P, 9RES, 3.3K, 2 PERCENT	11237	750-101-R3.3K
R4-6	000331	RES, CARB COMP, 330 OHM, 5 PERCENT 1/4W	81349	RC07GF331J
R7	080024	RES NETWORK, 6P, 5RES, 3.3K, 2 PERCENT	11237	750-61-R3.3K
R8	000180	RES, CARB COMP, 18 OHM, 5 PERCENT 1/4W	81349	RC07GF180J
R9	000560	RES, CARB COMP, 56 OHM, 5 PERCENT 1/4W	81349	RC07GF560J
R10	000331	RES, CARB COMP, 330 OHM, 5 PERCENT 1/4W	81349	RC07GF331J
R17-18	080057	RES NETWORK, 8P, 7RES, 100K, 2 PERCENT	11237	750-81-R100K
R19	000472	RES, CARB COMP, 4.7K, 5 PERCENT, 1/4W	81349	RC07GF472J
R50	080082	RES NETWORK, 10P, 9RES, 3.3K, 2 PERCENT	11237	750-101-R3.3K
R51-52	000102	RES, CARB COMP 1.0K 5 PERCENT 1/4W	81349	RC07GF102J
R53	000103	RES, CARB COMP, 10K, 5 PERCENT 1/4W	21793	RC07GF103J
R54	000332	RES, CARBON, 3.3K, 1/4W, 5 PERCENT	81349	RC07GF332J
SK2	601249	CONN, DIP, RIGHT ANGLE, 14-PIN	52072	CA-14SE-10RAC3-01
SK3	601582	CONN, RECEPTACLE, 24 PIN	00779	553811-4
SK4	R-23-5161	PLUG, RT. ANGLE, 2 ROW, 2 PIN	53878	929838-01-02
SW1	600814	SWITCH-SLIDE-6SPST	02660	31-010
(36)1	411820	PCB, GPIB (UNLOADED)	21793	411820
(41)1	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	530153-2
(42)1	601247	CABLE ASSY, 28 PIN	52072	CA-D28P02-28-1-TT-430
(45)2	611059	CONN, DIP, LOW PROFILE, 40-PIN	91506	240-AG39D
(46)2	516252	SCREW, PPH,SEMS ASSY,4-40X.312	78189	63-040545-25
(47)1	630010	HARDWARE KIT, STANDOFF, STUD MOUNT	00779	552533-3
(48)1	920524	SOCKET, IC, 24-PIN	52072	CA-24STSD-BC
(49)1	920891	SOCKET, 28-PIN	52072	CA-28S-TSD-BC
(50)1	R-11-1603	G.P.I.B. PLATE ASSY.	21793	R-11-1603

404386, OSCILLATOR ASSY., REV. C

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
J14	611056	CONNECTOR, CABLE, 5-PIN	21793	611056
(1)1	401822	PCB, DOUBLER (UNLOADED)	21793	401822
(2)1	454879	OSCILLATOR, 5 MHZ FREQ. STD	21793	454879
(4)A/R	500054	TUBING, SHRINK, .093 ID, BLK	29005	RNF-100-1-3/32
(6)2	610304	SPACER, .250D X .125 LG	21793	610304
(8)2	611074	SCREW, METRIC PAN HD., M3 X 10	21793	611074
(10)2	617102	WASHER, FLAT, #4, LIGHT SERIES	96906	MS15795-803
(11)2	617127	WASHER, LOCK, #4	88044	AN935C4
(13)A/R	500005	TUBING, SHRINK, .125 ID, BLK	29005	RNF-100-1-1/8
(15)A/R	500174	WIRE, TEFLON COAX	21793	500174
(17)A/R	524555	WIRE, TEFLON, STRANDED, 24 GA, GRN	21793	524555
(19)A/R	524929	WIRE, TEFLON, STRANDED, 24 GA, WHT/RED	21793	524929
(20)3	610777	CABLE TIE	16956	08-432
(22)1	611052	KEY, POLARIZING, PLUG	C0779	87077-1
(23)3	611053	TERMINAL, CRIMP	C0779	530553-2

401822, PCB ASSY., DOUBLER, REV. A

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1-9	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
D1-2	R-22-1029	DIODE, SILICON	14433	1N4149
L1	310151	CHOKE, 10 PERCENT, 100 UH	83125	DO100UH
Q1-2	200299	TRANS, PNP	04713	2N3906
Q3-5	200298	TRANS, NPN	04713	2N3904
R1	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-33 OHM-5 PCT
R2-3	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R4	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R5-6	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R7	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1.5K-5 PCT
R8-9	R-20-5798	RES, CHIP, 3.9K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.9K-5 PCT
R10	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1.5K-5 PCT
R11	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R12	R-20-5808	RES, CHIP, 39K, 1/8W, 5 PERCENT, 200V	65940	MCR18-39K-5 PCT
R13	R-20-5803	RES, CHIP, 15K, 1/8W, 5 PERCENT, 200V	65940	MCR18-15K-5 PCT
R14	R-20-5816	RES, CHIP, 330K, 1/8W, 5 PERCENT, 200V	65940	MCR18-330K-5 PCT
R15	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R16	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R17-18	R-20-5798	RES, CHIP, 3.9K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.9K-5 PCT
R19	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R20	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R21	R-20-5814	RES, CHIP, 51 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-51 OHM-5 PCT
T1-2	R-23-7149	TRANSFORMER	21793	R-23-7149
TP1	R-24-3537	TERMINAL ASSY.	21793	R-24-3537
(10)1	411822	PCB, DOUBLER (UNLOADED)	21793	411822
(58)3	R-24-3519	AV LUGS	19738	AVLUG1107/0208

R-18-1206, B.N.C. MOUNTING BOARD ASSY., REV. 1

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
SK19-20	R-23-5159	CONNECTOR, FEMALE, DUAL-ROW, 2 X 2 WAY	63878	929975-02
(1)1	R-15-0138	LABEL	21793	R-15-0138
(8)1	R-18-1206	P.B. BOARD, BNC MOUNTING (UNLOADED)	21793	R-18-1206
(10)3	R-23-3421	BNC SOCKET	24931	28JR175-7